# Thermal-Aware Physical Design Flow for 3-D ICs

**Jason Cong and Yan Zhang**
**UCLA Computer Science Department**
**{cong, zhangyan}@cs.ucla.edu**

## Abstract

3-D IC technologies have recently drawn great interest due to their potential performance improvement, power consumption reduction and heterogeneous components integration. One of the largest challenges in 3-D IC design is heat dissipation. In this paper we propose a thermal-aware physical design process for 3-D ICs, including floorplanning (*3DFP-T*), placement (*T3Place*) and routing (*TMARS*). Temperature optimization is considered during all three steps.

## 1. Introduction

Three-dimensional (3-D) IC technologies can significantly reduce interconnect length by stacking multiple device layers vertically. Therefore, 3-D IC technologies provide a great potential for improving the total wirelength [3], system performance, and power consumption [4]. Furthermore, 3-D IC technologies also provide a flexible way to carry out the system-on-chip (SoC) design by integrating heterogeneous components such as memory and logic circuits, radio frequency (RF) and mixed signal components, optoelectronic devices, etc.

One of the most critical challenges in 3-D IC design is heat dissipation, which has already posed a serious problem for 2-D IC designs [2]. The thermal problem is exacerbated in the 3-D cases for mainly two reasons: (1) the vertically stacked multiple layers of active devices cause a rapid increase in power density; (2) the thermal conductivity of the interlayer dielectric layers between the device layers is very low compared to silicon and metal. For instance, the thermal conductivity for epoxy, $k_{epoxy}$ is *0.05W/mK*, while $k_{silicon}$ is *150 W/mK* and $k_{copper}$ is *285 W/mK*. Therefore, the thermal issue needs to be considered during every stage of the 3-D IC design, including the three major steps of the physical design process: floorplanning, placement and routing.

A via that goes through a device layer is called a *through-the-silicon* via (TS via). TS vias are a new kind of physical object in 3-D ICs, and are usually fabricated using costly special technologies. Under the current technology, TS vias (pitch ≈5μm×5μm) are usually much larger than a regular via (pitch≤0.5μm×5μm). The routing resource for TS vias is limited since there are always large obstacles at device layers. TS-vias are effective "heat pipes" for power dissipation, while regular vias and wires have very little effect on circuit temperature because of their tiny sizes and the horizontal direction. Therefore, in addition to the macro blocks/cells and the netlist, thermal TS vias have become another kind of important object that the physical design process needs to deal with.

There has been a fair amount of work on physical design tools for 3-D IC designs. Early approaches [10][11] are mostly simple partition-based approaches, where the 3-D design is divided into smaller 2-D designs and the 2-D components are then designed using the existing 2-D design tools. Later on, people began to consider thermal problems in 3-D physical design tools [1][7][8][9].

In this paper we propose a thermal-aware 3-D physical design flow. During every step in the flow, temperature optimization is considered, as well as conventional design metrics such as chip area, wirelength, etc. The remainder of this paper is organized as follows. Section 2 presents the overall thermal-aware 3-D physical design framework and the related thermal models. Section 3 presents the thermal-aware 3-D floorplanning algorithm. Section 4 presents the transformation-based thermal-aware 3-D placement algorithm which tries to make use of the current 2-D placement tools. Section 5 presents the thermal-aware 3-D multilevel routing system with via planning. Finally, we conclude this paper and discuss future work in Section 6.

## 2. Thermal-Aware 3-D IC Physical Design Framework and Thermal Models

Figure 1 illustrates the proposed thermal-aware 3-D physical design system. The design flow is composed of three major steps: floorplanning, placement and routing. The macro blocks or cells are first placed into the stacked device layers and the interconnects are then routed. The individual tool components in the design flow can interface with each other through OpenAccess [16]. The shaded boxes represent the verification modules that are needed for a complete design flow, including the thermal simulations tools, timing analysis tools, layout verification tools, etc.

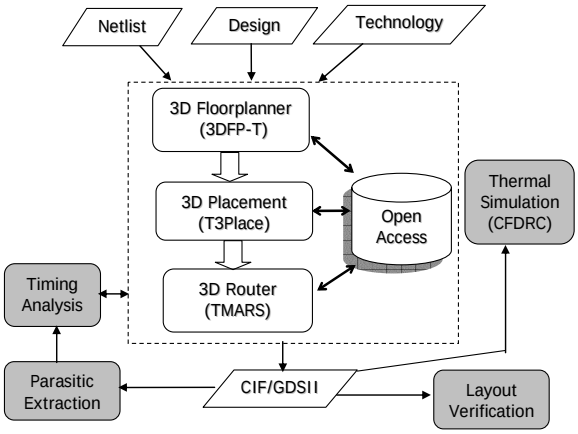


**Figure 1. The Proposed 3-D IC Physical Design Flow**

The thermal problem is one of the largest concerns in 3-D IC circuit design. The thermal target of 3-D circuit design is to constrain the maximum on-chip temperature within a given value, and/or to reduce/eliminate hot spots. During the physical design process, the on-chip temperature is primarily affected by two factors (assuming each heat source is of fixed power density): (1) the placement of the heat sources, i.e., the macro blocks/cells, and (2) number and locations of the TS vias.

TS vias are usually large in size and costly to fabricate. Large numbers of the TS vias will degrade both the yield and performance of the chip. Therefore, the number of TS vias in the circuit needs to be minimized as long as the temperature constraint is met.

A thermal-aware 3-D physical design process decides the following: (a) the locations of all macro blocks/cells, (b) the number and positions of TS vias, and (c) the routing paths of all nets.

The thermal TS via planning is considered during both the placement and the routing processes. During the floorplanning/placement process, whitespaces are reserved for thermal TS vias according to the heat dissipation need. The number and distribution of all thermal vias is carefully planned to satisfy both the thermal and routability requirements during 3-D routing.

### 2.1 Thermal Resistive Network Model

For temperature profiling, we use the fast compact resistive thermal model proposed by CFDRC [6]. Figure 2 shows the resistive model of a 5-layer circuit, with the whole chip stack being divided into an array of tile stacks. Each tile is connected to its neighbor at the same layer by lateral thermal resistors, $R_{lateral}$. Within each tile stack, a thermal resistor is modeled for each device layer. The power density value at each node is treated as a current source, and the temperature at each node is equivalent to the voltage at that node. The temperature can be calculated after solving the resistive network. The resistive network model is quite accurate. Because of the long runtime, it is primarily used for temperature verification.

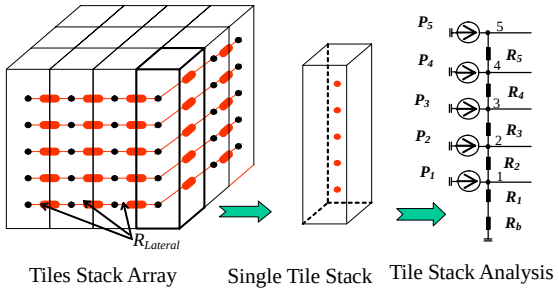


**Figure 2. 3-D Compact Resistive Network Thermal Model**

### 2.2 Analytical Resistive Chain Thermal Model

If only first-order heat dissipation is considered within a tile stack, then the temperature increase can be written in an Elmore-delay-like formula. For example, the temperature at node 4 of the vertical tile stack in Figure 2 is:

$$T = \sum_{i=1}^{4}(R_i \sum_{j=i}^{4} P_j) + R_b \sum_{i=1}^{4} P_i = \sum_{i=1}^{4}(P_i \sum_{j=1}^{i} R_j) + R_b \sum_{i=1}^{4} P_i \quad (1)$$

The fast analytical model is used during the optimization iterations in floorplanning and placement. For each tile stack, we calculate the temperature of the top layer node, which will be the hottest node in that tile stack, and the highest temperature will be put into the cost function for temperature optimization. Also, Equation (1) shows a way of deriving the rough thermal cost of assigning a cell/macro block with power density *P* to layer *i*

$$C_T(P,i) = P_i \sum_{j=1}^{i} R_j$$

## 3. Thermal-Aware 3-D Floorplanning (3DFP-T)

We extended the TCG [14] floorplanning representation data structure and proposed a *Combined Bucket and 2-D Array* (CBA) representation for 3-D floorplanning. A TCG structure is used to represent each layer, and a bucket structure is posed on the circuit stack to speed up block query by (*x*,*y*) coordinates. In each bucket, the indexes of the blocks that intersect with the bucket are stored, no matter which layer the block is located in. In the meantime, the indexes to all buckets that overlap the block are also stored in each block. The complexity to generate such a bucket is O(n), while the complexity to update it is normally O(1) since we only need to update the related grids each time we perform one operation on the representation and we don't need to reconstruct the bucket.

Based on the CBA representation, we use the simulated annealing (SA) engine to optimize the following weighted cost.

$$C = \alpha \cdot wl + \beta \cdot area + \gamma \cdot v + \lambda \cdot T \quad (2)$$

where *wl*, *area*, *v*, and *T* are normalized wirelength, chip area, number of TS vias and maximum temperature, respectively.

Once a floorplan configuration is generated, the power dissipation at each tile is calculated and the temperature at each tile can then be profiled by the thermal model to evaluate the cost function Equation (2). In this way, we can control the maximum on-chip temperature to a reasonable level by using cost function Equation (2) to guide the SA engine.

During the floorplanning process, thousands or even millions of different configurations are evaluated. To speed up the thermal profiling, we use a hybrid thermal model made up of the resistive thermal network model (Section 2.1) and the fast first-order resistive chain-based thermal model (Section 2.2). The fast model is used for the iterations within one SA temperature and the accurate model is called when the SA temperature drops to correct the error introduced by the rough thermal model.

The resistive network thermal model and its solver are provided by CFD Research Corporation (CFDRC). We have tested our algorithm on MCNC benchmarks and GSRC benchmarks. Four device layers are assumed for all experiments in the remainder of the paper. Each block is randomly assigned with a power density value between $10^5$(w/m$^2$) and $10^7$(w/m$^{2)}$. Table 2 shows the basic characteristics of the circuits that we used to the proposed floorplanner, 3DFP. The results of the conventional 2-D floorplanning are also listed for comparison. Table 3 compares the results of the wirelength-driven 3-D floorplanner, 3DFP, and the thermal-aware version, 3DFP-T. Compared to 2-D results, 3DFP can reduce the total wirelength by about 90%. Compared to 3DFP, 3DFP-T can reduce the on-chip maximum temperature by 45% with the cost of a 28% larger area, 14% longer wirelength, 25% more TS via number and 4.4× runtime. The runtime overhead is primarily caused by repeated iterations of the thermal modeling.

## 4. Thermal-Aware 3-D Cell Placement (T3Place)

T3Place is a novel method for generating 3-D thermal-aware placement from the existing 2-D placement results through a two-step procedure: *3-D transformation* and *layer refinement*. For 3-D transformation, we propose *local stacking transformation* (LST) and *folding-based transformation*. The layer assignment refinement procedure is based on a relaxed conflict-net (RCN) graph representation.

T3Place has several advantages over the other algorithms that generate a 3-D placement directly: (1) The existing 2-D placement core engine can be easily reused and an efficient transformation from a 2-D placement to a 3-D placement enables us to leverage the existing high-quality 2-D placers, such as Kraftwerk [12], MPL [5], etc.; (2) A simple yet effective thermal cost is derived for temperature optimization during layer assignment; (3) A flexible TS via number and wirelength tradeoff is offered by different transformation schemes and the parameter settings in the RCN graph-based layer assignment, which allows our algorithm to be used for different 3-D technologies.

Figure 3 shows the framework of T3Place. Components with a dashed boundary are existing tools that we use. A 2-D wirelength- and/or thermal-driven placer generates a 2-D placement first. The quality of the final 3-D placement will highly depend on the initial placement. The 2-D placement will then be transformed into a legalized 3-D placement according to the given 3-D technology. During the transformation, wirelength and temperature minimization are considered. A refinement process through layer assignment is then carried out to further reduce the TS-via number and bring down the maximum on-chip temperature. Finally, a 2-D detailed placer further refines the placement result for each device layer.

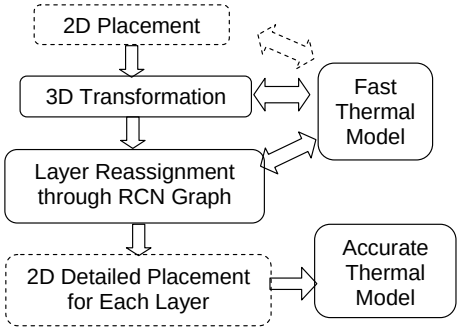


**Figure 3. T3Place Framework**

*Local stacking transformation* (LST) consists of two steps, *stacking* and *legalization*. In the stacking step, neighboring cells are formed into *k*-layer cell stacks (*k* is the number of device layers) and the 2-D wirelength is minimized. The legalization step minimizes maximum on-chip temperatures and TS via numbers through simultaneous row and layer assignment. The result of LST is a legalized 3-D placement.

A *folding-based* transformation will fold the original 2-D placement like a piece of paper without cutting off any parts of the placement. The advantage of folding is that the distance between any two cells will not increase and the total wirelength is guaranteed to decrease. TS vias are introduced to the nets crossing the folding lines (shown as the dashed lines in Figure 4). Figure 4 shows one folding scheme, which is folding once at both *x* and *y* directions.

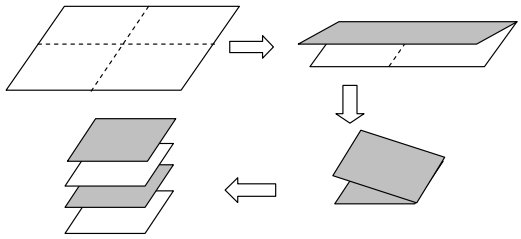

**Figure 4. Transformation Through Folding**

To further reduce the TS via number and maximum temperature, a *relaxed conflict-net* (RCN) graph, as shown in Figure 5, is used for layer reassignment. In the RCN graph, cells and TS vias are nodes. One via node is assigned for each net and all cells of that net are connected to it through a *net* edge. A *conflict* edge is created between the cells that overlap with each other. Conflict edges are assigned with infinity costs. The resulting graph is a directional acyclic graph. The cost of a layer assignment is the sum of the total via number and the thermal costs of all cells. The layer assignment heuristic will first generate a large sub-tree of the RCN graph. Then, a dynamic programming optimization method can be used to find the optimal solution for each induced sub-tree of the graph. This process can be repeated to further improve the quality of results.

T3Place is based on MPL [5], a multilevel force-directed 2-D placement tool. The placement benchmarks (from [13]) are listed in Table 1. We separately report the 2-D wirelength, "WL," and the number of TS vias. The wirelength results of the wirelength-driven T3Place are also listed in Table 1. Compared to 2-D mPL, T3Place can reduce the wirelength to over 2.2× under a four-layer technology.

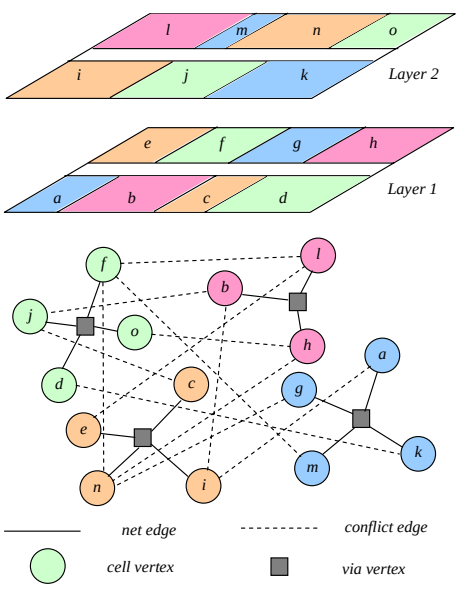


**Figure 5. Relaxed Conflict-Net Graph**

We also compared the two transformation methods: LST and folding. Folding can achieve very few TS via numbers — over 90% fewer than those of LST with a cost of 81% longer wirelength.

**Table 1. Benchmark characteristics and wirelength comparison of T3Placer and 2-D mPL5**

| Circuit | #Cell | #Net | 2-D mPL5 WL | WL-Driven T3Place WL |
|---|---|---|---|---|
| ibm01 | 12282 | 11507 | 5.19E+06 | 2.44E+06 |
| ibm02 | 19321 | 18429 | 1.44E+07 | 6.77E+06 |
| ibm03 | 22207 | 21621 | 1.37E+07 | 6.32E+06 |
| ibm04 | 26633 | 26163 | 1.67E+07 | 8.15E+06 |
| ibm05 | 29347 | 28446 | 4.23E+07 | 2.00E+07 |
| ibm06 | 32185 | 33354 | 2.20E+07 | 9.55E+06 |
| ibm07 | 45135 | 44394 | 3.73E+07 | 1.65E+07 |
| ibm08 | 50977 | 47944 | 3.94E+07 | 1.81E+07 |
| ibm09 | 51746 | 50393 | 3.46E+07 | 1.42E+07 |
| ibm10 | 67692 | 64227 | 6.82E+07 | 3.11E+07 |
| ibm11 | 68525 | 67016 | 5.02E+07 | 2.09E+07 |
| ibm12 | 69663 | 67739 | 7.58E+07 | 3.64E+07 |
| avg. | | | 100% | 44.34% |

Finally, thermal-aware T3Placer and T3Placer without temperature optimization are compared. LST transformation is used in both schemes. The thermal-aware T3Placer can reduce the maximum on-chip temperature by 30% on average with a cost of 6% more TS vias and 7% longer wirelength.

## 5. Thermal-Aware 3-D Multilevel Routing with Thermal Via Planning (TMARS)

The thermal-driven 3-D routing with a TS-via planning problem can be described as follows, given the following input:

1) The target 3-D IC technology, including design rule, height and thermal conductivity of each material layer

2) A 3-D circuit placement or floorplan result with whitespace reserved between blocks for interlayer interconnects

3) A given maximum temperature $T_0$, e.g. 80°C

route the circuit according to the connecting rule and design rule, so that the weighted cost of wirelength and the total TS-via number is minimized.

The size and thermal conductivity disparity between TS-vias and the regular signal wires and vias makes it difficult to handle them together. An individual step of TS-via planning also gives us more control over the temperature of the circuit, since the TS-vias are planned directly instead of being planned through shortest-path searching.

We propose TMARS, a multilevel 3-D routing system with a novel thermal TS via planning algorithm. With a more global view and the planning power of a multilevel planning scheme, the TS via planning step can effectively optimize temperature and wirelength through direct planning of the TS vias.

### 5.1 TMARS Framework

The multilevel framework has a powerful planning capability. To fully utilize the existing framework, we integrate the TS-via planning and the wire planning into one multilevel planning framework. The new thermal-driven 3-D routing system, shown in Figure 6, has a “downward pass,” where the routing resources are estimated using a weighted area sum model, and the routing resources for local nets are reserved at each level. Moreover, the thermal-related information, such as the average power density of each tile, is also computed during the coarsening process. During the initial routing stage, a 3-D Steiner tree is

generated for each multipin net. The Steiner tree heuristic starts from a minimum spanning tree (MST), and a path-to-path maze-searching engine is applied to each edge of the initial MST. Steiner edges are generated when the searching algorithm touches the existing edges of the tree before the target point. Since the maze-searching algorithm can find the shortest path around obstacles, the problem of many huge obstacles on the device layers can be solved. Then, the number of thermal TS-vias that need to be inserted is estimated through binary search. The upper bound of thermal TS-via (TTS via) numbers that can be inserted into each device layer is estimated by the amount of whitespace between the blocks. From our experience, the TTS-via number can be determined in fewer than ten iterations. During each refinement stage, the TTS-vias are refined first to minimize wirelength and maximum temperature. After TS-via refinement, the wires are also refined according to the refined TS-vias. The multilevel routing system communicates with the thermal model throughout the whole planning process. Before TTS-via planning, the latest thermal profile will be provided by the thermal model. The thermal model reads in the tile structure and the TS-via number at each tile and returns a temperature map with one temperature value assigned to each tile.

### 5.2 Alternating Direction Via Planning (ADVP)

We developed a very effective TS-via minimization technique, named multilevel alternating direction TTS-via planning (*m-ADVP*) algorithm. We formulate the TTS-via minimization problem as a constrained nonlinear programming problem (NLP) and solve it by solving a sequence of simplified TS-via planning sub-problems in alternating directions in a multilevel framework. *m-ADVP* iteratively distributes TTS-vias vertically and horizontally. The vertical TTS-via distribution is formulated as a convex programming problem with an analytical optimal solution for cases with no capacity constraint. We also use a set of shortest paths instead of the whole resistive network to speed up the heat flow calculation. The TS-via planning algorithm is integrated with a multilevel routing framework. At every refinement level, signal TS-vias are assigned for wirelength minimization before the TTS-via assignment.

To test TMARS, we use the results generated by our 3DFP without temperature optimization, so the effects of the thermal TS via insertion is more obvious. We also assume a required temperature of 77C. The final temperatures are calculated by the accurate full resistive thermal model at the finest level.

We first compared the wirelength-driven 3-D router (MARS-3D) to the thermal-aware 3-D router with the simple TS via planning heuristic of inserting TS vias proportional to the temperature distribution (TMARS+VPPT). With thermal TS via insertion, TMARS can always reach the required temperature, which is only about 44% of the temperature generated by MARS-3D, with a 2% longer wirelength and a 76% longer runtime.

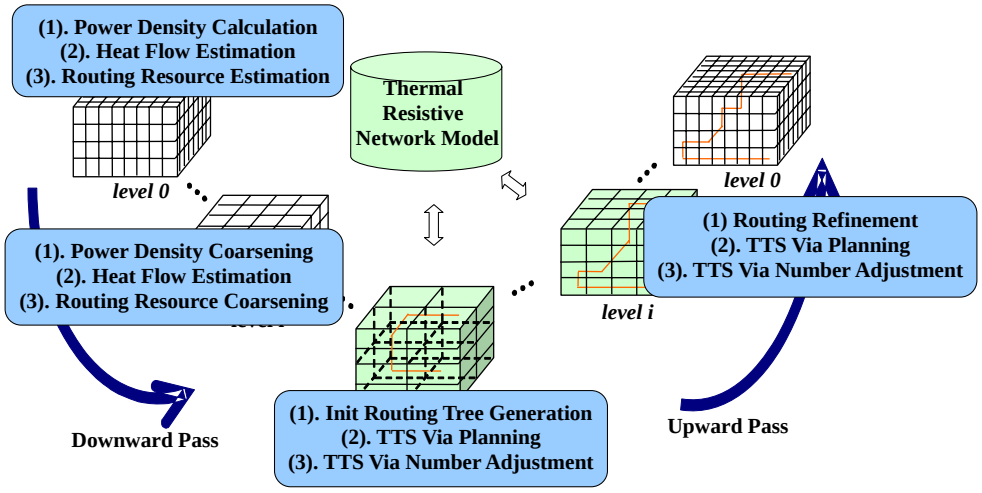


**Figure 6. Thermal-Driven 3-D Multilevel Routing System Framework**

Three different thermal TS via planning schemes — m-ADVP; the simple heuristic of multilevel VPPT, m-VPPT; and even distribution, EVEN — are compared in Table 4. All schemes are required to bring the temperature down to 77C. For the same temperature constraint, *m-ADVP* can reduce the total TS-via number by 69% over *m-VPPT*, and 3.6× over EVEN. We also used a conjugate gradient penalty function-based NLP solver package [15] to solve the TS via planning problem. Compared to directly solving the NLP, m-ADVP generates a similar number of TS vias with a 200× speedup in runtime.

The complete routing flow is finished by further wire planning and a grid-based detailed router. The results are shown in Table 5. The completion rate of a circuit is affected by the number of thermal TS-vias. Under the *m-ADVP* scheme, the router can reach the highest completion rate of 96.3%. When a design is hard to route, the router will take a longer runtime to search in a larger space for a solution. Figure 7 is the final layout generated by 3DFP and TMARS for ami33.

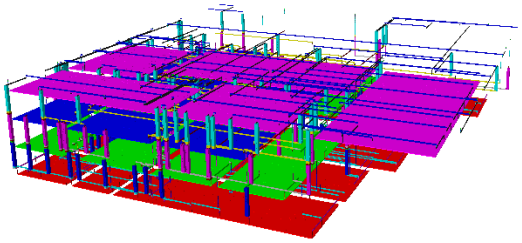

**Figure 7. Sample Final Layout of ami33**

## 6. Conclusions

We developed a complete thermal-aware 3-D physical design flow and applied it to an automatic 3-D architecture evaluation flow. Temperature, as well as conventional design objectives, like area, wirelength, etc., is considered during every step in the flow. Thermal TS vias are inserted and carefully planned to help heat dissipation without occupying too much routing resource. Our proposed approaches are very effective in controlling temperature. For the benchmarks that we tested, 3DFP-T can reduce the temperature by 45%, T3Place can reduce the chip temperature by about 30%, and TMARS can always control the temperature within the required range. For more information on this work, our project website is at http://cadlab.cs.ucla.edu/three_d/3dic.html.

There are many interesting topics in the 3-D physical design area. First, design tools that simultaneously consider multiple design constraints such as performance, signal integrity, thermal issues and routability are necessary for real 3-D circuit designs. Second, in order to generate a routable placement with reasonable maximum temperature, TS via numbers and locations should be considered in the early physical design steps, such as floorplanning and placement.

## 7. Acknowledgements

The authors wish to thank Dr. Marek Turowski and Mr. Patrick Wilkerson from CFD Research Corporation (CFDRC) for the compact resistive network thermal model. This research is partially supported by DARPA under contract DAAH01-03-C-R193, MARCO/DARPA GSRC, and NSF under grants CCF 0430077 and CCF-0528583.

## 8. References

[1] C. Ababei, Y. Feng, B. Goplen, H. Mogal, T. Zhang, K. Bazargan, and S. S. Sapatnekar, "Placement and Routing in 3D Integrated Circuits," *IEEE Design & Test of Computers*, Vol. 22, No. 6, pp. 520-531, November-December, 2005.

[2] K. Banerjee, "Thermal Effects in Deep Submicron VLSI Interconnects," (invited tutorial) *IEEE International Symposium of Quality Electronic Design*, 2000.

[3] K. Banerjee, S. Souri, P. Kapur, and K. Saraswat, "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *Proceedings of the IEEE*, 89(5):602-633, May 2001.

[4] B. Black, D. W. Nelson, C. Webb, and N. Samra, "3D Processing Technology and its Impact on IA32 Microprocessors," *Proceedings of IEEE International Conference on Computer Design*, pp. 316-318, 2004.

[5] T. Chan, J. Cong, and K. Sze, "Multilevel Generalized Force-directed Method for Circuit Placement," *Proceedings of the International Symposium on Physical Design*, pp. 185-192, San Francisco, CA, April, 2005.

[6] CFD-ACE+ Module Manual, Vol. I, Version 2002.

[7] J. Cong, J. Wei, and Y. Zhang, "A Thermal-Driven Floorplanning Algorithm for 3D ICs," *Proceedings of the International Conference on*

*Computer-Aided Design*, pp. 306-313, November, 2004.

[8] J. Cong, and Y. Zhang, "Thermal-Driven Multilevel Routing for 3-D ICs," *Proceedings of the Asia South Pacific Design Automation Conference*, pp. 121-126, January, 2005.

[9] J. Cong, and Y. Zhang, "Thermal Via Planning for 3-D IC's," *Proceedings of the 2005 IEEE/ACM International Conference on Computer Aided Design*, pp. 745-752, San Jose, CA, November, 2005.

[10] S. Das, A. Chandrakasan, and R. Reif, "Design Tools for 3-D Integrated Circuits," *Proceedings of the 2003 Conference on Asia South Pacific Design Automation*, pp. 53-56, 2003.

[11] Y. Deng , and W. Maly, "2.5D System Integration: A Design Driven System Implementation Schema," *Proceedings of the 2004 conference on Asia South Pacific Design Automation*, pp. 450-455, 2004.

[12] D. Hill, "Method and System for High Speed Detailed Placement of Cells Within an Integrated Circuit Design," *US Patent 6370673*, 2001.

[13] http://er.cs.ucla.edu/benchmarks/ibm-place/

[14] J.-M. Lin and Y.-W. Chang, "TCG: A Transitive Closure Graph Based Representation for Non-Slicing Floorplans," *Proceedings of ACM/IEEE Design Automation Conference (DAC-2001)*, pp. 764-769, Las Vegas, NV, June 2001.

[15] W. Naylor, and B. Chapman. http://www.willnaylor.com/wnlib.htm.

[16] http://openeda.si2.org/

**Table 2. MCNC and GSRC Benchmarks**

| Circuit | #block | # Net | #Pin | 2-D Area | 2-D WL |
|---|---|---|---|---|---|
| ami33 | 33 | 123 | 42 | 1.24E+06 | 50290 |
| ami49 | 49 | 408 | 22 | 3.82E+07 | 663010 |
| n100 | 100 | 885 | 1873 | 210378 | 180413 |
| n200 | 200 | 1585 | 3599 | 214349 | 393644 |
| n300 | 300 | 1893 | 4358 | 206954 | 394358 |
| Avg. | | | | 3.54 | 1.9 |

**Table 3. 3-D Floorplanning Results**

| Circuit | 3DFP | | | | | 3DFP-T | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Area | WL | #Via | T(C) | RT(s) | Area | WL | #Via | T(C) | RT (s) |
| ami33 | 3.44E+05 | 23475 | 111 | 470.7 | 23 | 4.25E+05 | 21853 | 104 | 191.9 | 170 |
| ami49 | 1.27E+07 | 465053 | 203 | 258.7 | 86 | 1.61E+07 | 550381 | 233 | 195.4 | 250 |
| n100 | 51736 | 90143 | 752 | 391.4 | 313 | 6.65E+04 | 115315 | 1052 | 172.7 | 689 |
| n200 | 50055 | 175866 | 1361 | 322.6 | 1994 | 6.91E+04 | 218739 | 1991 | 180.5 | 3415 |
| n300 | 75294 | 230175 | 1568 | 372.8 | 3480 | 9.46E+04 | 283377 | 2314 | 202 | 8649 |
| Avg. | 1 | 1 | 1 | 1 | 1 | 1.28 | 1.14 | 1.25 | 0.54 | 4.4 |

**Table 4. Comparison of Different TS-Via Insertion Approaches**

| Circuits | mADVP | | | | mVPPT | | | | EVEN | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | T(C) | #Via | Area Ratio | RT(s) | T(C) | #Via | Area Ratio | RT(s) | T(C) | #Via | Area Ratio | RT(s) |
| ami33 | 77 | 1282 | 0.025 | 1.55 | 77 | 1801 | 0.035 | 1.76 | 77.1 | 2315 | 0.045 | 1.62 |
| ami49 | 77 | 20956 | 0.009 | 13.5 | 77 | 43794 | 0.018 | 12.15 | 76.9 | 166366 | 0.068 | 16.17 |
| n100 | 77 | 11887 | 0.015 | 7.66 | 77.8 | 22211 | 0.028 | 8.31 | 76.8 | 30853 | 0.039 | 7.54 |
| n200 | 77 | 13980 | 0.018 | 12.24 | 77.2 | 18835 | 0.024 | 10.89 | 77.1 | 30346 | 0.039 | 12.21 |
| n300 | 77 | 17646 | 0.013 | 20.44 | 77.1 | 30161 | 0.022 | 21.73 | 76.9 | 57342 | 0.042 | 22.42 |
| Avg. | | 1 | 1.60% | 1 | | 1.11 | 1.80% | 0.98 | | 3.55 | 4.70% | 1.06 |

**Table 5. Final Routing Results**

| Circuits | TMARS+mADVP | | TMARS+mVPPT | | TMARS+EVEN | |
|---|---|---|---|---|---|---|
| | C.R. | RT(s) | C.R. | RT(s) | C.R | RT(s) |
| ami33 | 100.00% | 7.38 | 100.00% | 6.92 | 100.00% | 7.45 |
| ami49 | 97.24% | 954.2 | 94.40% | 1173.8 | 79.40% | 1835.3 |
| n100 | 94.26% | 4136.9 | 88.30% | 6210.7 | 61.60% | 15161.8 |
| n200 | 94.00% | 14922.5 | 94.00% | 13340.5 | 68.20% | 46352 |
| n300 | 99.13% | 1431 | 91.70% | 4110.8 | 58.00% | 13618.1 |
| Avg. | 96.93% | 1 | 93.68% | 1.49 | 73.44% | 3.84 |