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A Millimeter-Wave CMOS Transceiver With Digitally Pre-Distorted PAM-4 Modulation for Contactless Communications

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***Abstract*— This paper presents a millimeter-wave (127 GHz) CMOS transceiver with a digital pre-distortion capable PAM-4 modulator for contactless communications. The transmitter upconverts PAM-4 modulated baseband signals through a free-running 127-GHz oscillator and single-balanced mixer, and it delivers PAM-4 modulated carrier signals to a folded-dipole antenna, which is designed on a FR408HR substrate. The receiver's low-noise amplifier provides a 10-dB gain, and the self-mixer downconverts carrier-modulated PAM-4 signals to baseband signals without the necessity of carrier synchronization. The PAM-4 modulator pre-distorts the baseband signals and corrects the non-linear characteristics of the transmitter's upconversion mixer and the receiver's downconversion self-mixer. Designed and fabricated in a 65-nm CMOS process, the demonstrated system transfers 20 Gb/s of PAM-4 modulated data through a 1-mm air gap and consumes 79.5 mW (transmitter: 50.8 mW and receiver: 28.7 mW) of power under a 1.2-V supply, achieving a 3.98-pJ/bit energy efficiency. The communication distance is extended to 3 cm by inserting a dielectric waveguide between the same transceiver.**

***Index Terms*— Contactless communication, dielectric waveguide, digital pre-distortion (DPD), impulse response, millimeter-wave transceiver, non-linearity, PAM-4.**

I. Introduction

CONTACTLESS communications aim to realize multi-tens of gigabits-per-second (Gb/s) data transfers between digital electronics by placing paired devices in close proximity, typically within a few millimeters of each other. Mechanical connectors in wire line communication systems (e.g., USB, High-Definition Multimedia Interface (HDMI), and DisplayPort) often create frequency notches in the main signal paths, degrading the communication bandwidth [1].

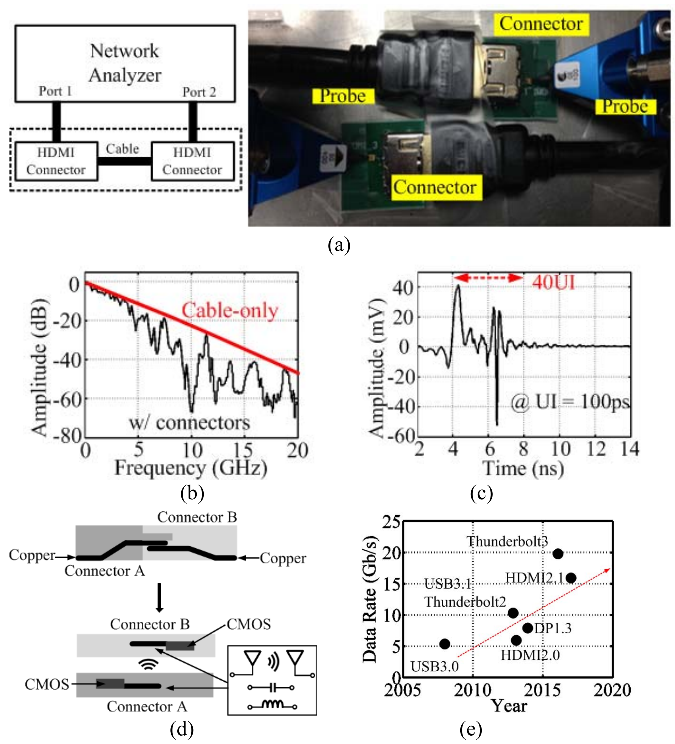

Fig. 1. (a) Mechanical connector and measurement setup using VNA. (b) Measured transmission characteristic. (c) Measured impulse response. (d) Mechanical versus contactless connector concept. (e) Recent trend in the wire line communication standard.

To study such non-ideal effects, an HDMI connector's transmission characteristic is measured as illustrated in Fig. 1(a). A cable-only configuration experiences a low-pass characteristic, but the measured frequency response in Fig. 1(b) exhibits multiple frequency notches after inserting mechanical connectors. The corresponding impulse response of the measured channel is plotted in Fig. 1(c) to emphasize the necessity of equalization.

Currently, two different research branches are engaged in developing contactless communications to replace mechanical

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connectors as depicted in Fig. 1(d): carrier-modulated wireless transmissions [2]–[8] and inductive/capacitive coupling schemes [9]–[11].

The inductive/capacitive coupling systems are attractive due to their compact transceiver architecture, but they face difficulties in bandwidth scalability and a tradeoff between coupler size and communication distance. Carrier-modulated wireless systems provide avenues with which to scale bandwidth and reduce coupling antenna size by selecting appropriate carrier frequencies. However, they consume relatively large amounts of power to generate carrier signals and useful gain at millimeter-wave frequencies. To overcome such disadvantages, most research has focused on compact-transceiver-driven modulations such as amplitude-shift keying (ASK) [3], [4], on-off-keying (OOK) [2], [5]–[8], and frequency-shift keying (FSK) [12], [13]. Indeed, the OOK-modulated 60-GHz CMOS transceivers reported in [6]–[8] and [14]–[16] have led to the commercialization of contactless connectors, supporting data rates up to 6 Gb/s for detachable laptops and smartphone applications [17]. However, according to the wire line standard survey shown in Fig. 1(e), the communication bandwidth nearly doubles every 3–5 years, which means that the existing solutions encounter bandwidth scalability barriers imposed by the bandwidth-density inefficient ASK/OOK modulations. A dual-carrier (57 and 80 GHz) ASK modulation has been reported to double the bandwidth in [4] and [18], but they rely on a process/voltage/temperature sensitive carrier-recovery-less coherent detection.

This paper introduces millimeter-wave PAM-4 signaling enabled by a digital pre-distortion (DPD) technique to utilize bandwidth efficiently and continue scaling communication bandwidth.

In particular, a 127-GHz non-coherent transceiver integrated with a DPD-based PAM-4 modulator is designed to demonstrate the feasibility of such a concept [19]. The implemented system discards phase domain modulations and eliminates carrier recovery circuitries by employing a free-running oscillator in the transmitter (TX) and an envelope detecting self-mixer in the receiver (RX). The DPD cancels non-linear effects yielded by up/downconversion for the intended PAM-4 signaling.

II. Air-Coupling Design

A. PCB Dielectric Constant Measurement

Critical design parameters such as the dielectric constant and loss tangent are typically unavailable at millimeter-wave frequencies from printed circuit board (PCB) vendors. For instance, the Isola substrate datasheet offers the aforementioned data only up to 10 GHz [20]. Adopting the exact same procedure presented in [21], a sequence of PCB dielectric constant measurements, shown in Fig. 2(a), is conducted on various thicknesses (3, 5, 7, 10 μm) of FR4HR substrates. For each substrate thickness, microstrip transmission lines with 50-Ω characteristic impedance (Z_0) are designed based on the datasheet. Then, two different physical lengths of transmission lines are fabricated, as shown in Fig. 2(b). The electrical length difference (ΔL_e) between the two transmission lines are measured up to 67 GHz via a vector network analyzer (VNA),

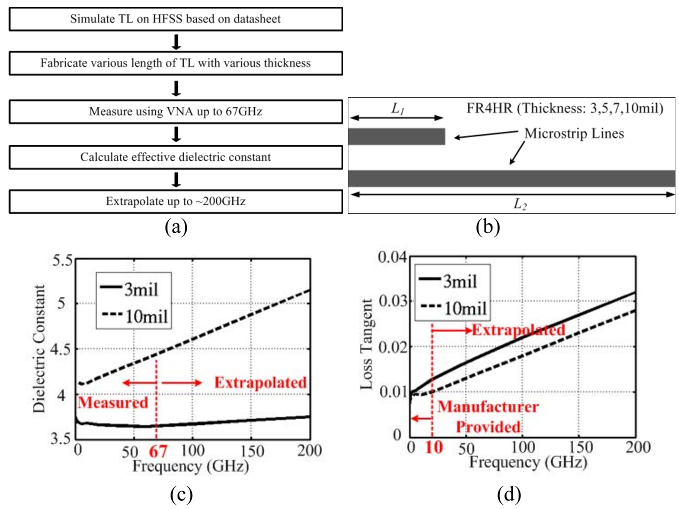


Fig. 2. (a) PCB dielectric constant measurement procedure. (b) Top view of two different physical lengths of transmission line. (c) Measured and extrapolated dielectric constant. (d) Extrapolated loss tangent.

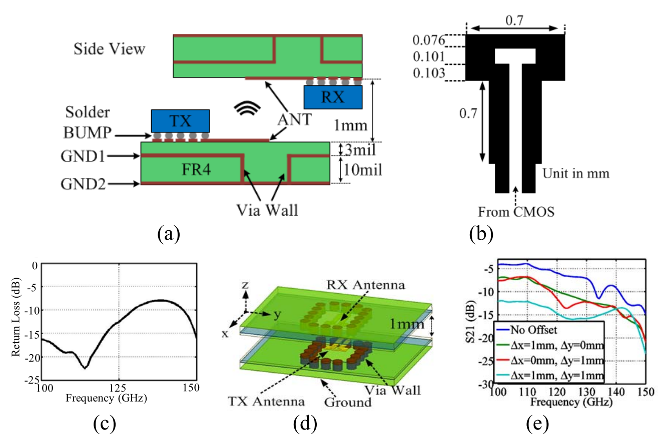


Fig. 3. (a) Side view of chip-to-PCB assembly diagram and PCB structure. (b) Detailed antenna dimension. (c) Simulated return loss. (d) Air-coupling simulation setup on HFSS. (e) Simulated transmission performance.

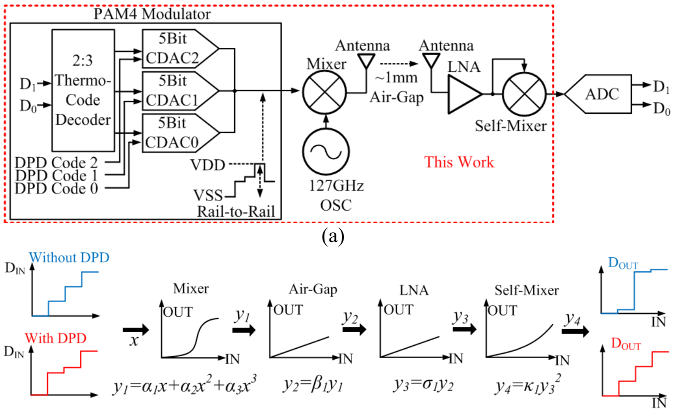
TABLE I
Measured and Extrapolated Dielectric Constant of PCB Substrate

Resin (%)	Thickness (mil)	Width (mil)	ε_r @10GHz (Meas.)	ε_r @60GHz (Meas.)	ε_r @100GHz (Extrap.)	ε_r @150GHz (Extrap.)
63	3	6	3.68	3.64	3.67	3.71
57	5	10.2	3.89	3.93	3.96	4
51	7	14.5	3.86	4.01	4.13	4.28
54	10	20.7	4.12	4.39	4.61	4.87

and the effective dielectric constant ($\varepsilon_{\mathrm{eff}}$) is calculated as

$$\Delta L_e = \sqrt{\varepsilon_{\mathrm{eff}}}(L_2 - L_1) \tag{1}$$

where L_1 and L_2 are the physical lengths of the longer and shorter transmission lines, respectively. The dielectric constant ε_r for each substrate is calculated based on the measured $\varepsilon_{\mathrm{eff}}$ and expressions provided in [22]. Several measured data points are listed in Table I. The dielectric constant beyond 67 GHz is extrapolated up to 200 GHz, and the dielectric constants of 3- and 10-mil substrates are plotted in Fig. 2(c). Based on this data, substrate profiles with



(a)

(b)

Fig. 4. (a) System block diagram. (b) System concept with and without DPD.

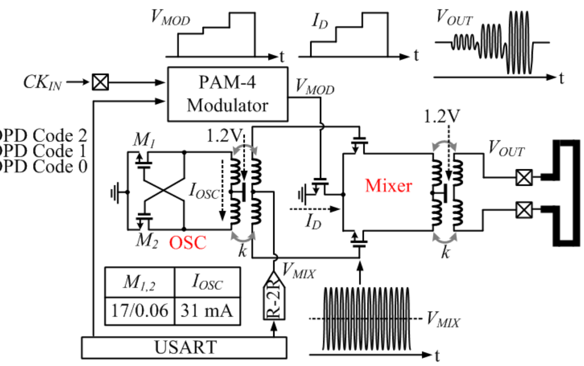


Fig. 5. Schematic of transmitter.

±10% discrepancies are also generated to compensate for the measurement/extrapolation inaccuracies. In Fig. 2(d), the loss tangent data are extrapolated from datasheet up to 200 GHz.

B. Antenna Design

Coupling antenna structures are designed based on the above data using High-Frequency Structural Simulator (HFSS) software. As illustrated in Fig. 3(a), a stack of 3- and 10-mil substrates with a ground plane underneath is chosen. The ground plane at 13 mil depth, which is approximately a quarter-wavelength ($\lambda/4$) at operating frequencies, produces constructive interference [23]. The optimized antenna dimension from all substrate profiles is described in Fig. 3(b). The CMOS TX and RX are assembled through a flip-chip process mainly because of its attenuation and impedance matching advantages over the wire-bond process. After the antenna's folded dipole strips are designed for the 100-Ω differential input impedance, another ground layer is placed at 3 mil depth to insert a feeding transmission line with a 100-Ω differential characteristic impedance. Between the 3- and 13-mil depth substrate, a via-wall is formed by placing a via at every 6 mil around the antenna pattern to contain electromagnetic (EM) energy in the case of multi-channel considerations. The simulated return loss in Fig. 3(c) presents greater than 50 GHz of antenna bandwidth. To understand the link performance through a 1-mm air gap, a duplicate set is copied vertically, as shown in Fig. 3(d). According to simulations in Fig. 3(e), the 1-mm air-coupling channel causes 7-dB loss at 127 GHz, and a 1 mm alignment offset along the x-/y-axis contributes 10 dB of extra attenuation.

III. System Concept

The system block diagram of a 127-GHz CMOS transceiver with DPD PAM-4 modulation is shown in Fig. 4(a). The short-distance communication implies a much lower channel attenuation and lower dynamic range than conventional wireless systems, such as cellular or Wi-Fi. This property allows essentially the utilization of a self-mixer-based non-coherent receiver. The self-mixer typically requires relatively high input power to generate a useful output swing due to its severe conversion loss. To support wideband communications, only a single-stage low-noise amplifier (LNA) is designed at the RX front end. The major benefit of the above strategy comes from low-power operations as the self-mixer performs most efficiently in the sub-threshold region without the necessity of a local oscillator (LO).

Considering the poor RX sensitivity and channel attenuation studied in Fig. 3(d), the TX's output power is targeted at 0 dBm. Due to poor power efficiency at millimeter-wave frequencies, power amplifiers are discarded in the TX, indicating that the upconversion mixer is responsible for generating the target output power. The TX's output matching, upconversion mixer's headroom, and LO swing set the maximum current that can flowthrough the upconversion mixer to reach the targeted output power.

In terms of signal flow, the PAM-4 signals modulate the 127-GHz carrier signals through the upconversion mixer, and the TX sends the PAM-4 modulated carrier signals to the PCB antenna. The PAM-4 modulator employs capacitive-digital-to-analog-converters (CDACs) for low-power operation. The modulator consists of three-banks of 5-bit CDACs instead of a single DAC in order to cancel the system's non-linearity through the DPD. Each CDAC bank is responsible for the amplitude of one distinct data-eye opening. Each input/output characteristic of the system is expressed in Fig. 4(b), where x is the PAM-4 modulator's output voltage level, and α_1, α_2, α_3, β_1, σ_1, and k_1 are gain-/loss-related constants. The upconversion mixer experiences approximately a third-order polynomial non-linearity; the air-gap obeys Maxwell's equations (linear); the one-stage LNA exhibits a linear response as will be shown in Section V; and the self-mixer creates a square non-linearity. Consequently, equally spaced PAM-4 signals end up with unequal spacing at the RX output. To invert such system non-linear operations, the PAM-4 modulator pre-distorts its output level by exchanging capacitance between the three CDACs.

IV. 127-GHz CMOS Transmitter Design

The TX schematic is described in Fig. 5. A transformer-loaded cross-coupled pair generates 127-GHz carrier signals, and the 127-GHz carrier is coupled to the mixer's switching pair devices. The transformer isolates dc conditions between the oscillator and mixer; the primary coil's center tap is used for the oscillator's power supply, and the secondary coil's center tap is used for setting the bias point of the mixer's switching pair. The dc bias conditions are configured by 8-bit

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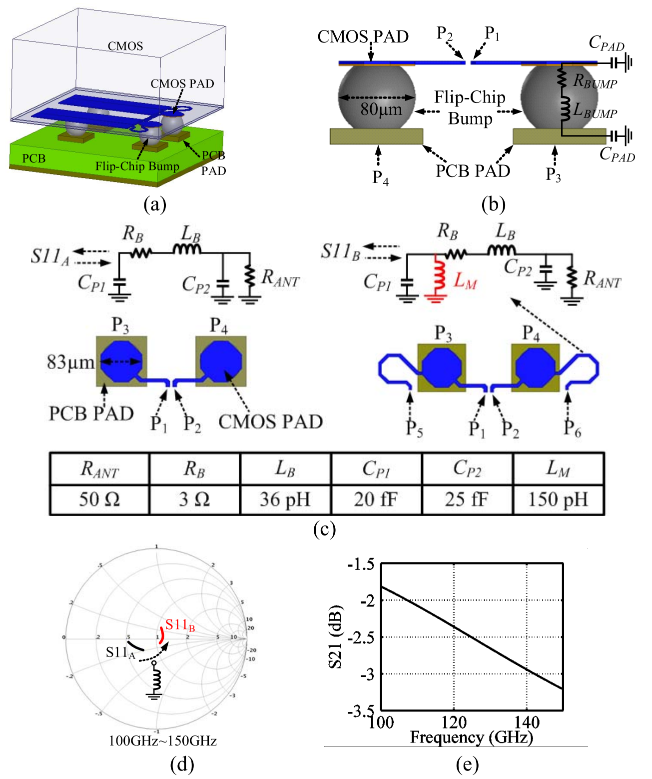

Fig. 6. (a) 3-D model of chip-to-PCB flip-chip assembly on HFSS. (b) Cross-sectional view of flip-chip bump and pads. (c) Top view of pad-to-pad interconnect and equivalent model. (d) Simulated return loss with and without shunt inductor. (e) Simulated transmission performance.

static R-2R DACs, and the corresponding digital codes are programed through the universal synchronous/asynchronous receiver/transmitter (USART). The PAM-4 modulator's output (V_{MOD}) is connected to the mixer's tail device to generate input-data-dependent PAM-4 modulated currents (I_D).

The DPD codes are also provided by the USART. The mixer's transformer transfers the PAM-4 modulated carrier signals to the PCB antenna.

A. CMOS-to-PCB Interface

A flip-chip process is applied to the CMOS-to-PCB assembly due to attenuation and impedance matching considerations at millimeter-wave frequencies. The interface characteristic is studied using HFSS software, and the 3-D model is captured in Fig. 6(a). The model includes the CMOS substrate, CMOS pads, flip-chip bump, PCB pads, and PCB substrate to capture attenuation through flip-chip bumps and substrate conduction. The cross-sectional view in Fig. 6(b) shows where ports P_1 to P_4 are excited in simulations. Ports P_1/P_2 interface with the output transformer on the CMOS side, and ports P_3/P_4 face the antenna on the PCB side. From this view, a simplified lumped-element model can be designed by conduction resistance in series with inductance and parallel capacitance on each side of the substrate. Based on the minimum flip-chip bump diameter requirement (80 μm), the diameters of the CMOS pads and PCB pads are designed to be 83 and 101.6 μm, respectively. The top view of such a configuration is shown in Fig. 6(c). To understand the

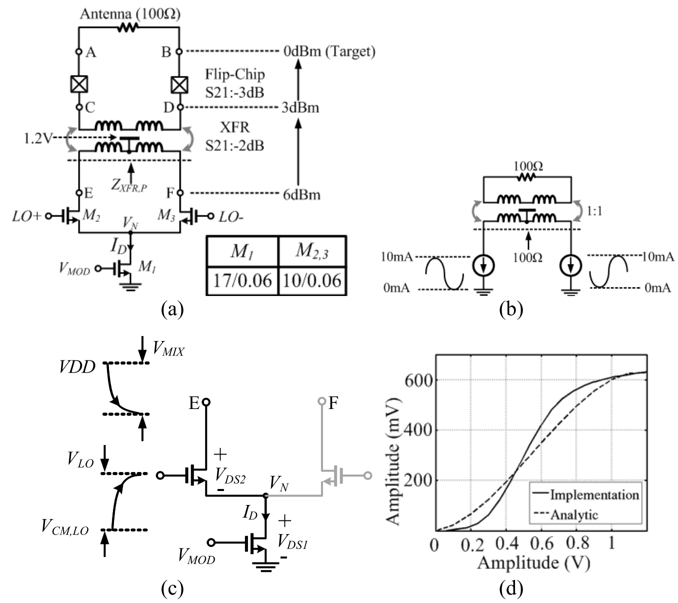

Fig. 7. (a) Schematic of upconversion mixer. (b) Ideal model of target performance. (c) Minimum required headroom and maximum output considerations. (d) Amplitude of mixer input versus amplitude of mixer output.

driving-point impedance behavior, differential ports are excited across P_1/P_2 while the antenna impedance (100 Ω) is loaded at ports P_3/P_4. Using the simulations outlined in Fig. 6(d), the driving-point impedance is altered by the reactance mentioned above.

To bring the input impedance back to 100 Ω (by rotating counterclockwise in the admittance plane), a shunt inductor is inserted in the network. As shown in Fig. 6(c), the shunt inductor can be designed with a ring which is tapped from the CMOS pad and connected to the ground through ports P_5/P_6. The resulting return loss $S11_B$ is plotted in Fig. 6(d). Finally, the transmission from the CMOS to PCB simulated in Fig. 6(e) shows 3-dB attenuation at 127 GHz with less than 2 dB in amplitude variation across 50 GHz of bandwidth.

B. Upconversion Mixer Design

As mentioned in Section III, the upconversion mixer alone must generate the necessary output power to satisfy the communication link budget. As shown in Fig. 7(a), the target output power at the antenna input port is set at 0 dBm. After counting attenuations from the flip-chip assembly in Fig. 6(e) and output transformer in Fig. 8(e), the target generated power at the mixer node E/F becomes 6 dBm, which is approximately a 2-V peak-to-peak voltage swing. Conceptually, the above condition can be established when the transformer's differential input impedance $Z_{\mathrm{XFR},P}$ is 100 Ω (1:1 ratio with 100-Ω loading), and the mixer current I_D is 10 mA, as illustrated in Fig. 7(b). From the implementation perspective in Fig. 7(c), the mixer output node E or F reaches $VDD - V_{\mathrm{MIX}}$ when the LO amplitude is at $V_{\mathrm{CM,LO}} + V_{\mathrm{LO}}$; then, I_D flows through either the E or F branch completely. To support such a current flow, a finite voltage drop appears across the switching pair and the current source devices, which means that $V_{\mathrm{DS1}} + V_{\mathrm{DS2}}$ sets the minimum voltage at node E or F. Therefore, the following two conditions can be considered

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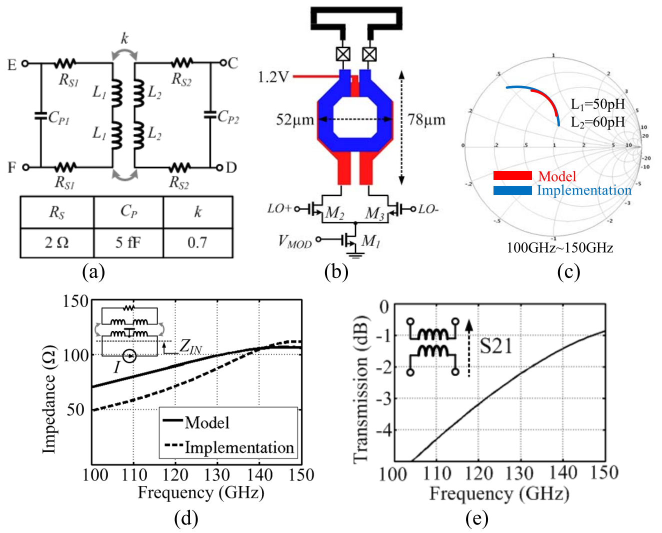

Fig. 8. (a) Lumpled-model-based transformer. (b) Transformer physical model. (c) Comparison of lumped model and physical model. (d) Driving point impedance on the primary coil side. (e) Simulated transmission performance of designed transformer.

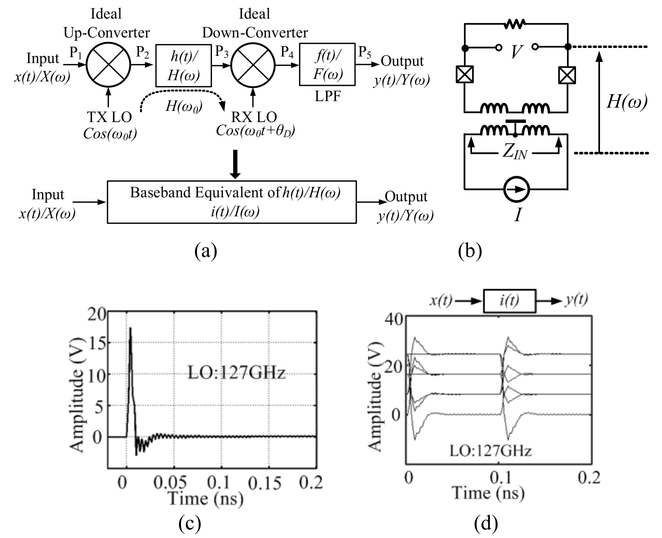

Fig. 9. (a) Block diagram of baseband equivalent impulse response analysis. (b) Transformer transfer function simulation. (c) Baseband-equivalent impulse response in time domain for 127-GHz LO. (d) Equivalent eye diagram for 127-GHz LO.

when determining design parameters:

$$V_{\mathrm{MIX,MAX}} = \begin{cases} VDD - V_{\mathrm{DS1}} - V_{\mathrm{DS2}}, \\ \quad \text{if } \dfrac{I_D \cdot Z_{\mathrm{XFR},P}}{2} > V_{\mathrm{DS1}} + V_{\mathrm{DS2}} \\ \dfrac{I_D \cdot Z_{\mathrm{XFR},P}}{2}, \\ \quad \text{if } \dfrac{I_D \cdot Z_{\mathrm{XFR},P}}{2} < V_{\mathrm{DS1}} + V_{\mathrm{DS2}}. \end{cases} \tag{2}$$

With a 10-mA current and 50-Ω single-ended impedance in Fig. 7(b), V_{MIX} is set at 0.5 V, thus the device size of $M_{1,2,3}$ is chosen to keep $V_{\mathrm{DS1}} + V_{\mathrm{DS2}}$ under 0.7 V. The largest $V_{\mathrm{DS1}} + V_{\mathrm{DS2}}$ occurs when the mixer's baseband port V_{MOD} is configured at the maximum voltage. In Fig. 7(d), V_{MOD} is swept from 0 to 1.2 V to observe how the carrier's amplitude at the TX output varies when the LO amplitude is 1 V. The current source device undergoes sub-threshold, saturation, and triode regions, and the TX generates a 630-mV peak-to-peak swing when $V_{\mathrm{MOD}} = 1.2$ V. Although the mixer suffers from non-linear operations, the monotonic increment indicates that a full-dynamic range at the baseband input port is necessary in order to maximize the PAM-4 signal's signal-to-noise ratio (SNR). An analytic input/output characteristic from Fig. 4(b) with $\alpha_1 = 0.1$, $\alpha_2 = 1$, and $\alpha_3 = -0.6$ is also plotted to model the non-linear behavior.

C. Output Transformer Design

The output transformer provides the required impedance that multiplies with the mixer current and transfers the PAM-4 modulated carrier signals to the antenna. A lumped model of the planar transformer is configured in Fig. 8(a). In this model, L is the inductance, R_S is the conductive resistance, and C_P is the capacitance between the differential feeding traces. Values of the coupling coefficient (k), R_S, and C_P are listed in the same configuration. To find optimal L values on the primary and secondary sides, each side of L is parameterized, and the resulting amplitude at 127 GHz is recorded at nodes E/F and C/D. The above simulation method is essentially the same as a load-pull simulation. The target 2-V peak-to-peak swing at the node E/F is achieved by using $L_1 = 50$ pH and $L_2 = 60$ pH. Based on the lumped model simulation, a physical transformer is designed as shown in Fig. 8(b). The comparison between the lumped model and physical model in Fig. 8(c) displays good agreement.

To calculate the driving-point impedance at the transformer input, an ac current source is excited differentially on the primary coil side, while the secondary coil is terminated with 100 Ω. The simulation result in Fig. 8(d) shows a 75-Ω input impedance at 127 GHz. In Fig. 8(e), the implemented transformer experiences a 3-dB attenuation from the primary to secondary coil side.

The output transformer is also responsible for supporting the necessary bandwidth at the target carrier frequency. A baseband-equivalent impulse response provides intuitions on the carrier-modulated system's bandwidth property [24], [25]. In Fig. 9(a), the transfer function $h(t)$ is the bandwidth limiting block. To apply the mathematical tool, the implemented transformer's transfer function is simulated by injecting an ac current source at the input of the transformer and measuring the voltage at the input of the antenna port, as shown in Fig. 9(b). That is, $H(\omega)$ is the combined response of Figs. 6(e) and 8(d) and (e). Using the simulated transformer's transfer function, the time-domain impulse response is calculated in Fig. 9(c). Since the time-domain impulse response is known, 20 Gb/s of PAM-4 modulated random signals are generated and convolved to create an eye diagram, as shown in Fig. 9(d). The transformer creates a time-domain peaking in this design.

V. 127-GHz CMOS Receiver Design

As shown in Fig. 10, the RX starts with an input transformer to transport incoming PAM-4 modulated carrier signals to the one-stage LNA. The LNA provides a 10-dB voltage gain

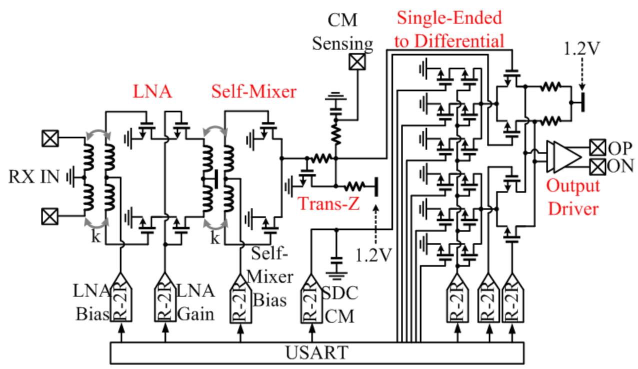

Fig. 10. Schematic of receiver.

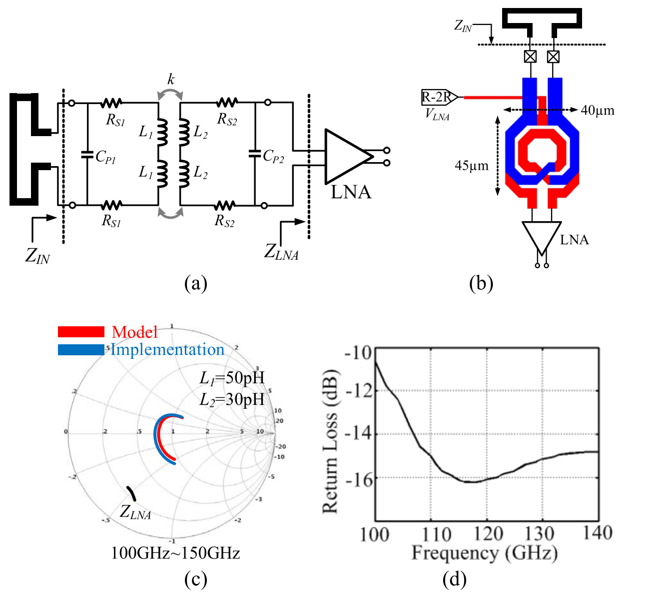

Fig. 11. (a) Equivalent input-stage model. (b) Physical input-stage transformer design. (c) Comparison of lumped model versus physical model. (d) Simulated return loss at RX input.

at 127 GHz. The amplified carrier signals are sent to the self-mixer via a transformer. The self-mixer generates currents that are comprised the PAM-4 baseband and 254 GHz of carrier content. The following transimpedance amplifier (TIA) converts the current into voltage and filters the 254-GHz carrier content. At the output of the self-mixer, an *RC* filter extracts the de-modulated PAM-4 signal's average dc content.

Because of the data pattern-dependent average dc level of PAM-4 signaling, an R-2R DAC feeds a constant common mode (CM) voltage to the single-ended-to-differential converter (SDC) after reading average dc values from the *RC* filter. In addition, to prevent a mismatch-oriented dc offset propagating through the SDC and following output drivers, an offset cancellation is embedded in the SDC using R-2R DACs and digitally controlled current sources.

A. Input Stage and LNA Design

A lumped transformer model is utilized for the input stage matching, as shown in Fig. 11(a). The same R_S and C_P values from Fig. 8(a) are used in this model. The LNA stage is loaded at the output of the secondary coil, and the input impedance of the LNA (Z_{LNA}) is plotted in Fig. 11(c). Based on

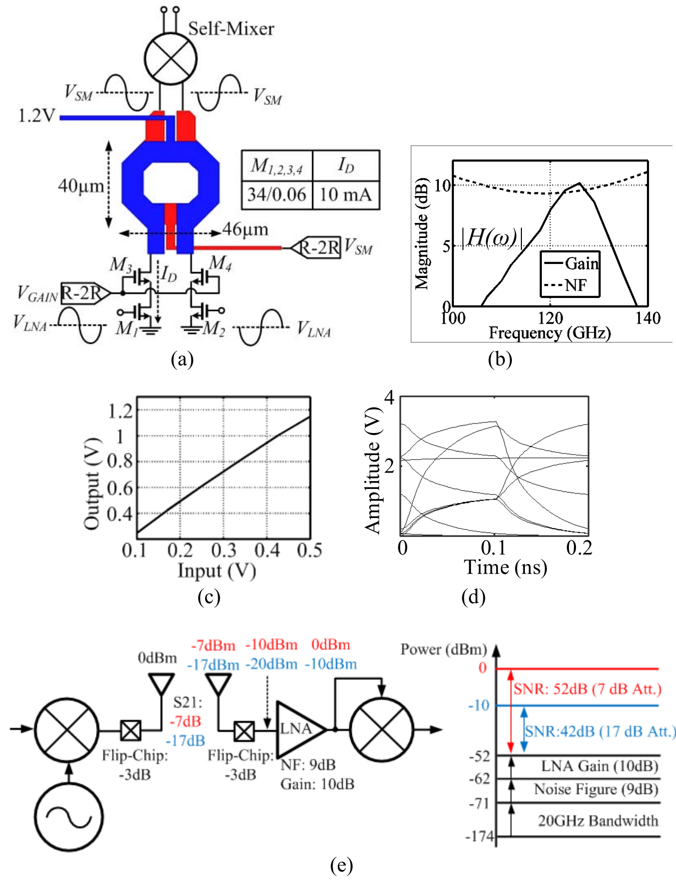

Fig. 12. (a) Physical transformer model for LNA. (b) Simulated LNA gain and NF. (c) Simulated LNA input and output characteristic. (d) Baseband equivalent eye diagram. (e) System block diagram with signal power level.

parametric simulations, the choice of 50 pH for L_1 and 30 pH for L_2 provides the input impedance shown in Fig. 11(c). Next, a physical transformer is designed in Fig. 11(b). The input impedance using the physical model matches to that of the lumped component model. The width of the metal layer in the RX input stage is narrower than in the TX output stage because no dc current flows through the RX input transformer. The return loss simulated in Fig. 11(d) shows below −10 dB beyond 40 GHz of bandwidth.

Using an identical method, the LNA's physical transformer is designed in Fig. 12(a). The supply voltage is fed through the primary coil's center tap, and the self-mixer's bias is provided by the secondary coil's center tap. The simulated gain and noise figure (NF) including the input-stage transformer are 10 and 9 dB at 127 GHz, respectively, as shown in Fig. 12(b). Because of the single-stage design, the LNA displays a linear input/output characteristic as shown in Fig. 12(c). Since the LNA's transfer function is ready, the baseband-equivalent impulse response is also applied to understand the bandwidth. When the carrier frequency is 127 GHz, a low-pass impulse response is expected. Just as in the TX case, 20 Gb/s of PAM-4 random signals are convolved with the time-domain impulse response, resulting in the noticeable inter-symbol interference (ISI) shown in Fig. 12(d).

To estimate the system SNR at the output of LNA, a system block diagram with signal power levels is summarized

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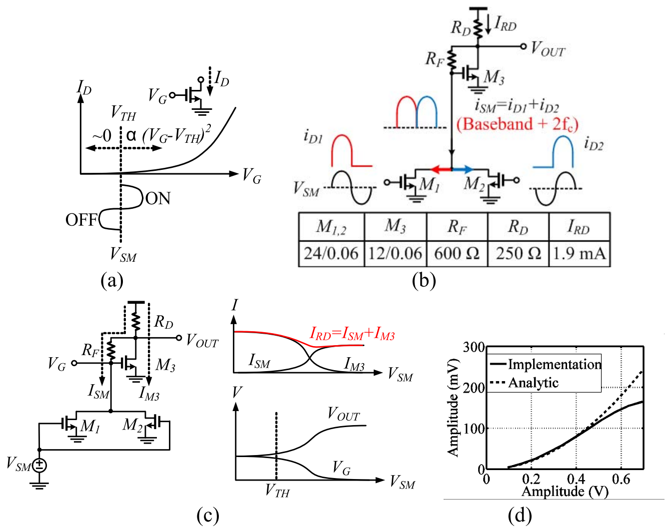

Fig. 13. (a) NMOS operation condition around threshold voltage. (b) Self-mixer operation. (c) Self-mixer dc operating condition. (d) Simulated self-mixer's input and output characteristics.

in Fig. 12(d). From Fig. 3(e), the channel experiences 7–17 dB of attenuation depending on how the TX and RX are aligned. The LNA receives −10 to −20 dBm power after passing through the flip-chip package. The desired signal, therefore, becomes 0 to −10 dBm at the output of LNA. For noise considerations, beginning from the noise floor at −174 dBm/Hz, the LNA integrates over 20 GHz of data bandwidth and contributes 9 dB of NF and 10 dB of gain. Therefore, the integrated noise floor is set at −52 dBm at the LNA's output. The SNR at the LNA's output is now calculated to be between 42 and 52 dB, depending on the channel conditions.

B. Self-Mixer Design

The self-mixer consists of two NMOS transistors, where each gate terminal is driven by each polarity of the carrier's differential signals. Drain nodes are tied together to combine currents generated from each transistor. As shown in Fig. 13(a), a transistor's drain current approaches zero when the gate bias (V_G) is below threshold (V_{TH}), and the drain current increases proportionally to the square of $V_G - V_{\mathrm{TH}}$ when the gate bias is above threshold, provided the transistor is in the saturation region. Using this property, the self-mixer's gate (V_{SM}) is biased at V_{TH} to act as a half-wave current rectifier. As shown in Fig. 13(b), the differential carrier signals produce half-wave rectified current through each drain terminal, and summed currents at the drain node result in the envelop of modulated carrier signals as well as the $2\omega_0$ content. The detailed dc operation condition is described in Fig. 13(c). When $V_{\mathrm{SM}} = 0$ V, the input transistors M_1 and M_2 are turned off, and the transistor M_3 is self-biased through the feedback resistor R_F. The gate and output voltages maintain the same potential initially, and the bias current flows only through M_3.

As V_{SM} increases, I_{SM} begins flowing through R_F, and V_G decreases to satisfy the operation conditions of transistors M_1 and M_2. Since V_G decreases, I_{M3} decreases as well. The current through R_D is equal to the sum of I_{SM} and I_{M3}. This current settles eventually at I_{SM} when the transistor M_3 is turned off. The output voltage V_{OUT} rises until I_{RD} reaches I_{SM} because $V_{\mathrm{OUT}} = VDD - I_{\mathrm{RD}} R_D$. To appreciate the input (millimeter wave) and output (baseband) characteristics, while the self-mixer's CM is biased at 0.32 V, the amplitude of the carrier modulated signal is varied, and the amplitude of the baseband output is measured at the output. In Fig. 13(d), the x-axis is the differential amplitude of carrier signal with the carrier frequency set at 127 GHz. The output amplitude increases proportionally to the square of the input swing initially and starts saturating after 0.5 V of input swing. This behavior is expected from Fig. 13(c), where V_{OUT} begins saturating, with I_{RD} reaching I_{SM}. An analytic expression from Fig. 4(b) with $k_1 = 0.5$ is plotted in Fig. 4(b) to show the square law relationship for the lower side of the input swing.

From Fig. 12(e), the carrier signal's amplitude at the self-mixer input ranges from 0.2 to 0.63 V, which results in a 20–150-mV baseband signal amplitude at the self-mixer output.

C. Self-Mixer Noise Contribution

The SNR study shown in Fig. 12(e) can be further extended to estimate the SNR at the self-mixer's output. Denoting $S(f)$ and $N(f)$ as the desired signal and noise signal, respectively, in the frequency domain, the normalized self-mixer output $M(f)$ is written as

$$\begin{aligned} M(f) &= (S(f) + N(f)) * (S(f) + N(f)) \\ &= S(f) * S(f) + 2S(f) * N(f) + N(f) * N(f) \\ &\cong S(f) * S(f) + 2S(f) * N(f) \end{aligned} \tag{3}$$

where the $*$ operator indicates a convolution. The $N(f)*N(f)$ term is neglected because the square of the noise power itself is much smaller than the other two terms. The desired signal and noise signal components are downconverted at the baseband with the magnitudes of $2S^2$ and $4SN$, respectively. The frequency components at $2f_c$ are filtered at the self-mixer's output. Therefore, the SNR at the self-mixer output (SNR_M) is

$$\mathrm{SNR}_M = \frac{2S^2}{4SN} = \frac{S}{2N} \tag{4}$$

which means that the ideal self-mixer's SNR degradation from input to output is 6 dB. In practice, the self-mixer's devices contribute broadband noise, and the self-mixer's non-linear input/output characteristic in Fig. 13(d) makes the NF dependent on the signal power level. The equivalent noise model is described in Fig. 14(a). The mean-square output noise voltage is calculated as

$$\overline{V}^2_{n,\mathrm{out}} = \left(\overline{I}^2_{n1} + \overline{I}^2_{n2} + \overline{I}^2_{n,Z_{\mathrm{TIA}}}\right) \cdot (Z_{\mathrm{TIA}}||r_{o1}||r_{o2})^2 \tag{5}$$

$$\overline{I}^2_{n1} = 4kT\gamma\, g_{m,M1} \tag{6}$$

$$\overline{I}^2_{n2} = 4kT\gamma\, g_{m,M2} \tag{7}$$

where Z_{TIA} is the TIA's input impedance, k is the Boltzmann constant, T is the temperature, and γ ($\cong 3$) is the device-dependent constant.

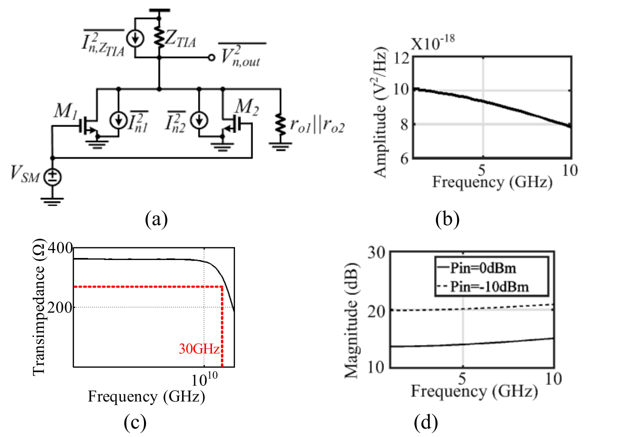

Fig. 14. (a) Self-mixer equivalent noise model. (b) Simulated self-mixer output noise. (c) Simulated transimpedance. (d) Simulated self-mixer NF.

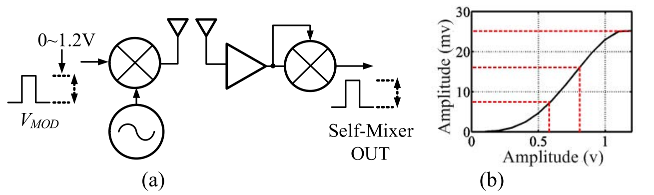

Fig. 15. (a) System non-linearity characterization. (b) Derived system non-linearity.

The TIA's input referred noise current is approximated as in [26]

$$\overline{I}^2_{n,Z_{\mathrm{TIA}}} = \frac{4kT\gamma}{g_{m,M3}R_F^2} + \frac{4kT}{g_{m,M3}^2 R_F^2 R_D} + \frac{4kT}{R_F}. \tag{8}$$

Using the simulated values $g_{m,M1} = g_{m,M2} = 7.4$ mS, $r_{o1} = r_{o2} = 1$ kΩ, $Z_{\mathrm{TIA}} = 360\Omega$, and $g_{m,M3} = 12$ mS, the mean-square noise voltage per 1 Hz at the output is calculated to be 3.4×10^{-17} V^2/Hz. The simulated self-mixer's output noise in Fig. 14(b) validates the noise calculation. Then, the noise is integrated over 30 GHz, which is 3-dB bandwidth of the TIA, as shown in Fig. 14(c), resulting in 1.02×10^{-6} V^2, or 1 mV$_{\mathrm{RMS}}$. Combining the device noise and signal-dependent downconverted noise contribution, the self-mixer's NF is simulated in Fig. 14(d), exhibiting a 13–20-dB NF over 10 dB of input power difference. Therefore, the SNR of the self-mixer's output is estimated to be between 22 (42-20) and 39 (52-13) dB depending on the channel misalignment. The analysis indicates that the 10-dB extra channel attenuation accrues a 17-dB SNR penalty instead of a 10-dB penalty, as is the case in coherent detection. This is one critical disadvantage of employing the self-mixer.

VI. PAM-4 Modulator Design

A. *Summary of System Non-Linearity*

The system experiences non-linear characteristics, as discussed in Sections IV and V. Using the expressions in Fig. 4(b), the overall input and output characteristics are plotted in Fig. 15(a) and (b). To summarize the process, at the TX mixer input, a baseband pulse is injected, and the pulse's amplitude is increased from 0 to 1.2 V. The modulated carrier signals travel through the air-coupling channel and LNA, which are considered to be linear, and they multiply themselves to return to a baseband pulse. Therefore, the overall input and output characteristics are recorded by sending a pulse and measuring the amplitude of self-mixer output pulse. As shown in Fig. 15(b), the system requires the TX input to be pre-distorted to achieve evenly spaced PAM-4 signals at the RX output.

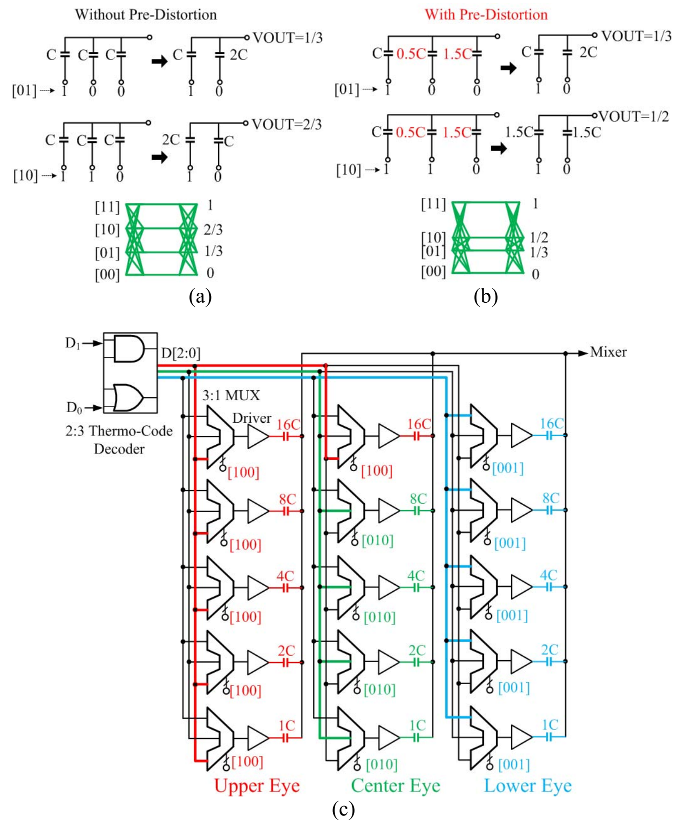

Fig. 16. (a) Capacitive divider without DPD. (b) Capacitive divider with DPD. (c) Configuration with DPD.

B. *PAM-4 Modulator Design and Time-Domain Simulations*

A 2:3 decoder splits the 2-bit PAM-4 data stream into a 3-bit thermo-code signal D[2:0], with each bit mapping to one of the three PAM-4 eyes. As shown in Fig. 16(a), each coded set of data drives each capacitor C. Each C represents one CDAC bank presented in Fig. 4(a). Depending on the input data, the output voltage is determined by a capacitive divider. For instance, when the input data is 01, the thermo-code becomes 001. Equivalently, the data drive C and 2C in series, where the output node is at 2C. This circuit yields 1/3 V. If the division ratio can be changed while the total capacitance remains the same across all three CDAC banks, the modulator's output voltage level can be pre-distorted as shown in Fig. 16(b). For example, if the 0.5C portion of the middle bank is given away to the right-side bank, the equivalent circuit now becomes 1.5C and 1.5C in series when the data is 10. This leads to 1/2 V instead of 2/3 V, widening the upper eye and reducing the middle eye. The difference between the two can be seen in the eye-diagram illustration. In the circuit implementation, each C can now be decomposed into

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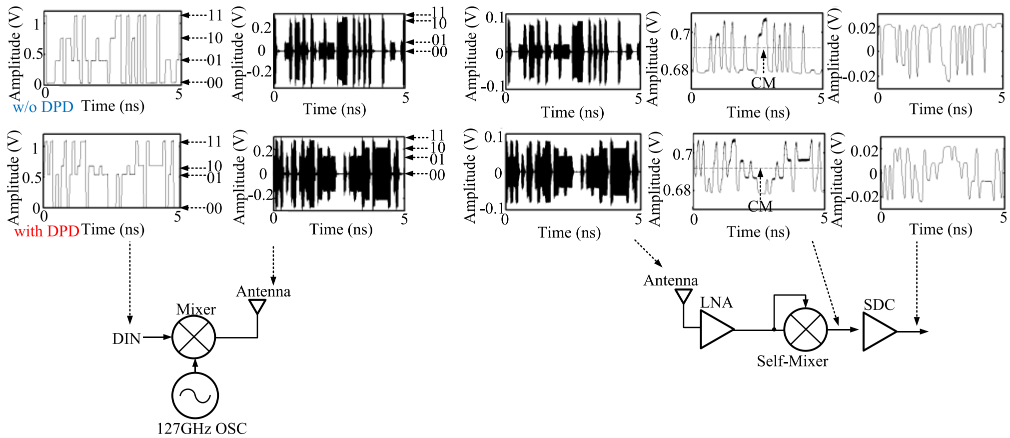
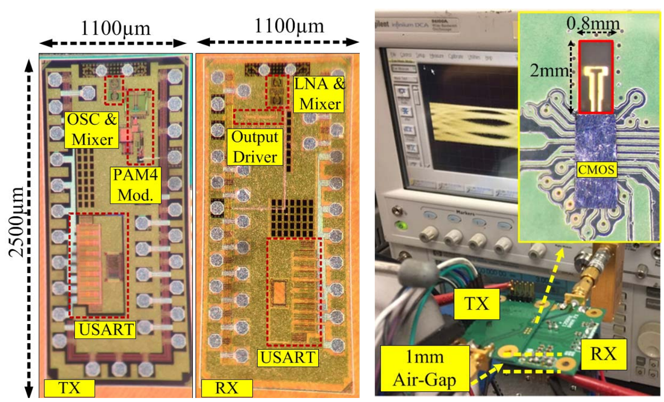
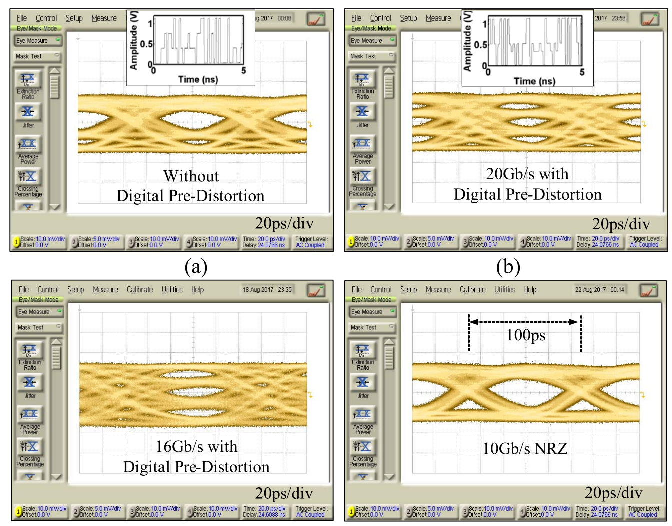


Fig. 17. Signal flow with and without DPD.



(a) (b)

Fig. 18. (a) Fabricated CMOS TX and RX. (b) Flip-chip assembled CMOS-chip/antenna and a 1-mm air-gap communication measurement setup.



(a) (b)

(c) (d)

Fig. 19. (a) Measured eye diagram without DPD. (b) Measured eye diagram at 20 Gb/s with DPD. (c) Measured eye diagram at 16 Gb/s with DPD. (d) Measured NRZ eye diagram at 10 Gb/s.

a binary-weighted capacitor array. An example is described in Fig. 16(c).

In the middle bank, for 16C, if the DPD code is set to 100 instead of 010, the most significant bit data drives an additional 16C from the middle bank on the top of its own capacitors in the left-side bank, resulting in an increased upper eye opening.

Time-domain simulations, as shown in Fig. 17, are conducted to prove the feasibility of the CDAC-based DPD at the target data rate of 20 Gb/s. Without the DPD, the input amplitude is populated equally. After the upconversion, the modulation depth at 127 GHz is distorted in such a way that data points 11 and 10 are hardly distinguishable. Propagating further to the receiver side, only three uneven levels can be detected because of the system's non-linearity. A DPD is applied to reduce the amplitude of the middle data, and now all four modulation depths are noticeable at the TX antenna port. Note that the modulation depths between the data are not equal at the TX antenna port; this is done to cancel the non-linear effect of the self-mixer in the RX. After amplifying and downconverting the DPD-applied PAM-4 modulated carriers, the recovered data exhibit all four levels evenly at the self-mixer output.

VII. Measurement

The prototype TX and RX are fabricated in a 65-nm CMOS process, as shown in Fig. 18(a). The data communication between TX and RX is tested by placing them 1 mm apart vertically, as shown in Fig. 18(b). The resulting eye diagrams are captured in Fig. 19(a)–(d). Without the DPD, the upper eye is closed completely, the center eye is wide open, and the lower eye is almost closed. This result is expected from Fig. 15(b), as the middle-level's output excursion is the largest with the same amplitude of the input level. Once the DPD is applied, all three levels open approximately equally, as shown in Fig. 19(b), realizing 20-Gb/s PAM-4 signaling at the 127-GHz carrier frequency. A lower speed at 16 Gb/s is also measured in Fig. 19(c). The DPD can also be configured to generate a non-return-to-zero (NRZ) signal, as shown in Fig. 19(d). While the DPD is applied for the NRZ signaling, the effect of the module offset is measured by recording the output voltage's amplitude in Fig. 20(a)–(d). In Fig. 20(a), the output voltage drops to 10 mV at 10-Gb/s NRZ when the air gap between the TX and RX increases to 5.5 mm without the x-/y-axis offset. In Fig. 20(b), the output voltage reaches 10 mV at 1.5 mm of the x-axis offset, whereas the amplitude arrives at the same value at 1 mm of the y-axis offset. The height is

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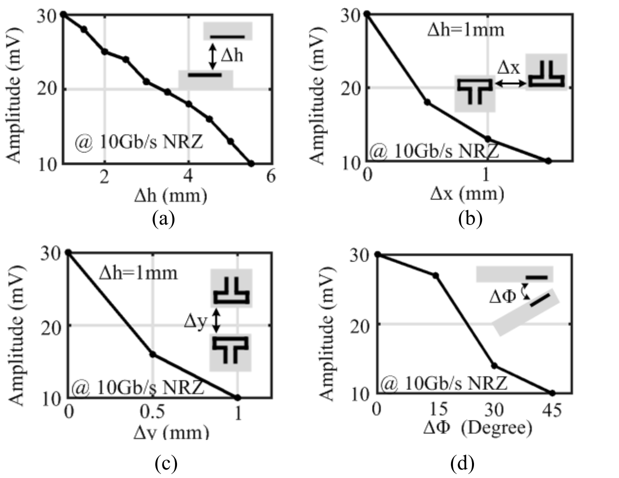

Fig. 20. (a) Output voltage versus height offset. (b) Output voltage versus x-axis offset. (c) Output voltage versus y-axis offset. (d) Output voltage versus angle offset.

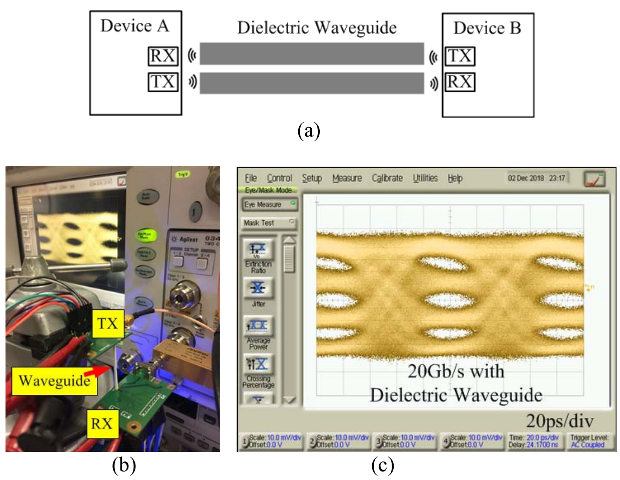

Fig. 21. (a) System configuration with dielectric waveguide. (b) Measurement setup with 3-cm dielectric waveguide. (c) Measured eye diagram with 3-cm dielectric waveguide at 20-Gb/s PAM-4 signaling.

fixed at 1 mm in both cases. The above experiment indicates that to formulate an array of contactless connectors for higher aggregate bandwidth, the minimum spacing between modules needs to be on the order of λ ($\lambda = 2.5$ mm at 120 GHz). In Fig. 20(d), the angle of contact is increased from 0° to 45° to demonstrate the contactless connector's flexibility. Using the exact same TX and RX, the communication distance is extended by inserting a dielectric waveguide, as shown in Fig. 21(a). Dielectric waveguides can sustain propagating modes if its dimensions are chosen properly (typically, a $\lambda/2$ cross section). In the past, data communications using circular waveguides [13], [14], [27] and dielectric ribbons [4] were demonstrated. In this design, a dielectric ribbon with a 2 mm × 0.8 mm cross-sectional diameter is placed on the top of the coupling antenna shown in Fig. 18(b).

As illustrated in Fig. 21(b) and (c), a dielectric ribbon extends the communication distance to 3 cm while establishing 20-Gb/s PAM-4 signaling.

To calculate the system bit-error-rate (BER), a constellation plot is constructed using the measured 20-Gb/s PAM-4 data

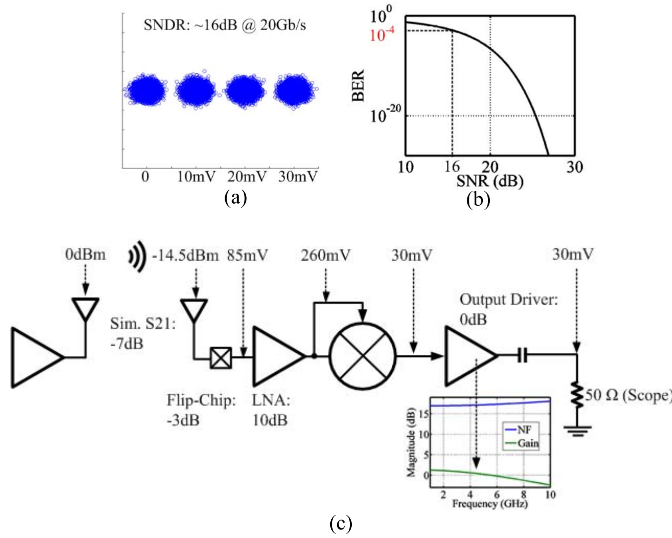

Fig. 22. (a) Reconstructed constellation from eye-diagram measurement. (b) BER versus SNR for PAM-4. (c) Summary of signal level.

TABLE II
SUMMARY OF POWER CONSUMPTION

		Power (mW)
TX	Oscillator	37.2
	Mixer	5.4
	CDAC	8.2
RX	LNA	24
	Self-Mixer	2.3
	Single-to-Diff Converter	2.4
	Total	79.5

from the oscilloscope, as shown in Fig. 22(a). The SNR is estimated to be 16 dB. The BER versus SNR for the PAM-4 signaling is plotted in Fig. 22(b). When the SNR is 16 dB, the BER is approximately 10^{-4}. PAM-4 systems typically require forward error correction (FEC) schemes to enhance the BER to at least 10^{-12} [28]. Therefore, the FEC will likely be necessary in future PAM-4-based contactless connector development.

To compare the measurement to the air-gap simulations in Fig. 3(d), signal levels for the 1-mm air-gap case without an x-/y-axis offset are described in Fig. 22(c). Beginning with the measured 30-mV amplitude, the self-mixer's output is estimated as 30 mV because the output driver provides a near-unity gain, as shown in Fig. 22(c). According to Fig. 13(d), to generate 30 mV at the self-mixer's output, the self-mixer requires 260-mV input swing. Considering the LNA's 10-dB gain and flip-chip bump's 3-dB loss, the received input power at the RX front end is calculated to be approximately −14.5 dBm. This result is 7.5 dB higher than the simulation result (provided the TX generates 0 dBm). The discrepancy can be caused by the TX output power, carrier frequency, PCB trace/substrate attenuation, or measurement accuracy. The same calculation for the 10-mV output from the x-/y-axis offset leads to a −19-dBm received input power at the RX front end. The measured 4.5 dB higher attenuation from the offset is within 2-dB accuracy compared to the simulation in Fig. 3(d).

The system power consumption is summarized in Table II. The 127-GHz oscillator in the TX and LNA in the RX

TABLE III
PERFORMANCE COMPARISON

	This Work	ISSCC 2012 [4]	ISSCC 2015 [13]	IMS 2017 [23]	ISSCC 2015 [9]	ISSCC 2013 [10]	JSSC 2016 [11]
Coupling Method	Antenna	Antenna	Antenna	Antenna	T-Line	Inductive	Capacitive
Carrier (GHz)	127	57 & 80	120	125	Baseband	Baseband	Baseband
Modulation	PAM-4	ASK	FSK	OOK	NRZ	NRZ	NRZ
Technology	65nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	0.18μm CMOS	14nm CMOS
Data Rate (Gb/s)	20	20	12.7	14	6	5.5	8
Power (mW)	79.5	137	59.7	60	36	198	32
FoM (pJ/bit)	3.98	6.85	4.7	4.3	6	36	4
BER	10^{-4}	$<10^{-12}$	10^{-12}	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$
Channel	Contactless/ Waveguide	Contactless/ Waveguide	Waveguide	Contactless	Contactless	Contactless	Contactless
Contactless Distance (mm)	1	5	N/A	2	1.11	5	0.8
Waveguide Distance (cm)	3	12	100	N/A	N/A	N/A	N/A

occupy the majority of system power consumption. The entire contactless communication system consumes 79.5 mW (TX: 50.8 mW and RX: 28.7 mW) while transporting 20 Gb/s of data. It results in a 3.98-pJ/bit energy efficiency. In Table III, previously reported results are summarized. The demonstrated system achieves the minimum energy per bit without counting the FEC implementation to meet the BER requirement.

VIII. CONCLUSION

This paper realizes a 127-GHz CMOS transceiver with a DPD PAM-4 modulation to achieve a 20-Gb/s data rate over a 1-mm air-coupling channel and 3-cm dielectric ribbon. The TX consists of a 127-GHz oscillator, upconversion mixer, and PAM-4 modulator. Extra power amplifiers are omitted because of bandwidth and power consumption considerations. The PAM-4 modulator is designed with three banks of CDAC to support the DPD. The 1-mm air coupling is established by sending EM energy through folded-dipole antennas, which are designed on FR4HR PCB. The PCB's dielectric constants are measured and extrapolated up to 200 GHz before designing the antennas. A dielectric ribbon is inserted between the antennas to extend the communication distance. The RX consists of a one-stage LNA and self-mixer, eliminating the necessity of carrier synchronization. The self-mixer creates a square-law non-linearity after self-multiplication. The measured eye diagrams prove the versatile capability of the DPD at millimeter-wave frequencies for multi-tens Gb/s short-distance communication systems.

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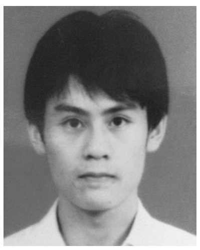
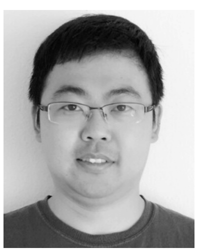
From 2010 to 2013, he commercialized the 60-GHz CMOS contactless communication at Waveconnex, Los Angeles, CA, USA. Since 2014, he has been designed CMOS system-on-chips (radar, radiometer, and spectrometer) with the Sub-Millimeter-Wave Technology Group, Jet Propulsion Laboratory, Pasadena, CA, USA. He is currently with the Radar Concept Group, Naval Research Laboratory, Washington, DC, USA.



Boyu Hu received the B.Sc. degree (Hons.) from Chu Kochen Honors College, Zhejiang University, Hangzhou, China, in 2008, the M.S degree from Zhejiang University in 2011, and the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2016.

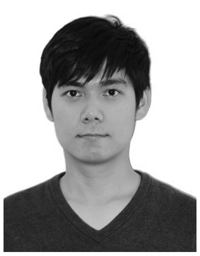
His research interests include high-speed/high-precision mixed signal integrated circuit and system, hardware mapping of complex signal processing algorithms and its related VLSI architecture and design, and hardware–software co-design for embedded systems.



Yuan Du (S'14) received the B.S. degree (Hons.) in electrical engineering from Southeast University, Nanjing, China, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2012 and 2016, respectively.

His research interests include designs of machine-learning hardware accelerator, high-speed wire line/SerDes, and RFICs.

Dr. Du was a recipient of the Microsoft Research Asia Young Fellowship in 2008, the Southeast University Chancellor's Award in 2009, and the Broadcom Fellowship in 2015.



Wei-Han Cho received the B.S. and M.S. degrees from National Tsing Hua University, Hsinchu, Taiwan, in 2008 and 2010, respectively, and the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2016.

Since 2016, he has been with Qualcomm Technology Inc., San Jose, CA, USA, where he is working on circuit design and IP development of the most advanced Wi-Fi technologies. His research interests include RF, mixed-signal, and analog circuits for wireless or wire line communication.

Rulin Huang (S'17) received the B.E. degree (Hons.) in electrical engineering from Zhejiang University, Hangzhou, China, in 2015, and the M.S. degree in electrical engineering from the University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 2017, where he is currently pursuing the Ph.D. degree.

He is currently with UCLA, where he is working on dielectric waveguide-based interconnect and beamforming arrays for 5G and automotive radar application.

Mr. Huang was a recipient of the UCLA Department Fellowship from 2015 to 2016 and the Broadcom Fellowship from 2016 to 2017.

Adrian Tang (M'10–SM'15) received the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2012.

He has over 15 years of CMOS/SiGe IC design experience in both research and commercial wireless environments with projects ranging from commercial Bluetooth and WLAN chipsets to millimeter-wave and terahertz chipsets for communication, radar, and spectrometer systems. In 2013, he joined Jet Propulsion Laboratory, Pasadena, CA, USA, where he was demonstrate sub-centimeter accurate millimeter-wave imaging radar in silicon technology with demonstrations at 144 and 155 GHz, pre-distortion in CMOS millimeter-wave transmitters above 150 GHz, and CMOS-based passive radiometers with enough sensitivity to support passive imaging, and he is currently leading the development of a wide range of CMOS system-on-a-chip (SoC) chipsets for planetary, earth science, and astrophysics space instruments.

Huan-Neng Chen is currently an Integrated Circuit Designer with Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

Chewnpu Jou received the B.S. and M.S. degrees from NTUEE, Taipei City, Taiwan, in 1982 and 1986, respectively, and the Ph.D. degree in high-frequency electronics from the State University of New York, Stony Brook, NY, USA, in 1991.

From 1991 to 1997, he worked as a RF Program Leader with the Industrial Technology Research Institute, Hsinchu, Taiwan, developing wireless front-end circuits and components for phones and Wi-Fi. From 1998 to 2001, he was an RF Senior Manager with United Micro Electronics, Hsinchu, Taiwan, leading RF-CMOS technology and design support. From 2002 to 2006, he was the Vice President with United Radio, Syracuse, NY, USA, delivering RFCMOS interface system-on-chip (SoC). In 2007, he served as RF Design Deputy Director with TSMC, Hsinchu. His experience encompasses RF front end to RF-SoC mainly in CMOS, low-temperature co-fired ceramics (LTCC), and silicon photonics. He has authored or co-authored over 20 IEEE publications and holds U.S. patents.

Dr. Jou has been served as an ISSCC TPC Member since 2011. He was a recipient of the 1997 Taiwan MOEA Best Project Award.

Jason Cong (M'89–F'00) received the B.S. degree in computer science from Peking University, Beijing, China, in 1985, and the M.S. and Ph.D. degrees in computer science from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 1987 and 1990, respectively.

From 2005 to 2008, he served as the Chair of the UCLA Computer Science Department, Los Angeles, CA, USA. He is currently a Distinguished Chancellor's Professor with the Computer Science Department, also with joint appointment from the Electrical Engineering Department, of the University of California at Los Angeles, Los Angeles, CA, USA, where he is also the Director of the Center for Domain-Specific Computing (CDSC), and the director of VLSI Architecture, Synthesis, and Technology (VAST) Laboratory. He has authored or co-authored over 400 publications. His research interests include novel architectures and compilation for customizable computing, synthesis of VLSI circuits and systems, and highly scalable algorithms.

Dr. Cong was elected to an ACM Fellow in 2008 and the National Academy of Engineering in 2017. He was a recipient of the 12 best paper awards, three 10-year most influential paper awards, and one inducted to the FPGA and Reconfigurable Computing Hall of Fame.

Tatsuo Itoh (S'69–M'69–SM'74–F'82–LF'06) received the Ph.D. degree in electrical engineering from the University of Illinois, Urbana, IL, USA, in 1969.

After working with the University of Illinois, SRI, Schaumburg, IL, USA, and the University of Kentucky, Lexington, KY, USA, he joined The University of Texas at Austin, Austin, TX, USA, as a Faculty Member, in 1978, where he became a Professor of electrical engineering in 1981. In 1983, he was selected to hold the Hayden Head Centennial Professorship of engineering at The University of Texas. In 1991, he joined the University of California at Los Angeles, Los Angeles, CA, USA, as a Professor of electrical engineering and holder of the TRW Endowed Chair in microwave and millimeter-wave electronics (currently Northrop Grumman Endowed Chair). He generated 70 Ph.D. students. He has authored or co-authored over 375 journals, 775 refereed conference presentations, and 43 books/book chapters in microwaves, millimeter waves, antennas, and numerical electromagnetics.

Dr. Itoh was elected as a member of the National Academy of Engineering in 2003. He is a member of the Institute of Electronics and Communication Engineers of Japan and Commissions B and D of USNC/URSI. He was a recipient of a number of awards including the IEEE Third Millennium Medal in 2000 and the IEEE MTT Distinguished Educator Award in 2000. He served as the Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUESfrom 1983 to 1985. He was the President of the Microwave Theory and Techniques Society in 1990. He was the Editor-in-Chief of IEEE MICROWAVE AND GUIDED WAVE LETTERS from 1991 to 1994. He was elected as an Honorary Life Member of MTT Society in 1994. He was the Chairman of Commission D of International URSI from 1993 to 1996. He serves on advisory boards and committees of a number of organizations. He served as a Distinguished Microwave Lecturer on microwave applications of metamaterial structures of IEEE MTT-S from 2004 to 2006.

Mau-Chung Frank Chang (S'76–M'79–SM'84–F'96–LF'18) is currently the President of National Chiao Tung University, Hsinchu, Taiwan, China. He is also the Wintek Chair Professor of electrical engineering with the University of California at Los Angeles, Los Angeles, CA, USA. His research interests include development of high-speed semiconductor devices and high-frequency integrated circuits for radio, radar, and imaging system-on-chip applications up to terahertz frequency regime.

Dr. Chang is a member of the US National Academy of Engineering, a fellow of the US National Academy of Inventors, and an Academician of Academia Sinica of Taiwan. He was a recipient of the IEEE David Sarnoff Award in 2006 for developing and commercializing GaAs HBT and BiFET power amplifiers for modern high-efficiency and high-linearity smart-phones throughout the past 2.5 decades.